

SSD1332

Advance Information

**96RGB x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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SSD1332

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1 GENERAL INFORMATION

The SSD1332 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 288 segments (96RGB) and 64 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1332 displays data directly from its internal 96x64x16 bits Graphic Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface or Serial Peripheral Interface. It has a 256 steps contrast control and 65K color control.

2 FEATURES

- Support max. 96RGB x 64 matrix panel
- Power supply: $V_{DD} = 2.4V - 3.5V$
 $V_{CC} = 7.0V - 18.0V$
- OLED driving output voltage, 16V maximum
- DC-DC voltage converter
- Segment maximum source current: 200uA
- Common maximum sink current: 50mA
- Embedded 96x64x16 bit SRAM display buffer
- 16 step master current control, and 256 step current control for the three color components
- Programmable Frame Rate
- Graphic Acceleration Command Set (GAC)
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature: -40 to 85 °C

3 ORDERING INFORMATION

Table 1 - Ordering Information

| Ordering Part Number | SEG | COM | Package Form | Reference | Remark |
|----------------------|-------|-----|--------------|-----------|---|
| SSD1332U1R1 | 96RGB | 64 | COF | Page 46 | <ul style="list-style-type: none">• 35mm film• 5 sprocket hole• 80 / 68 / SPI interface• SEG lead pitch 0.06mm• COM lead pitch 0.09mm |
| SSD1332T1R1 | 96RGB | 64 | TAB | Page 52 | <ul style="list-style-type: none">• 35mm film• 5 sprocket hole• Folding TAB• 80 / 68 / SPI interface• SEG lead pitch 0.06mm• COM lead pitch 0.09mm |
| SSD1332Z | 96RGB | 64 | COG | Page 8 | <ul style="list-style-type: none">• Min SEG pad pitch: 41.2 μm• Min COM pad pitch: 41.2 μm |

4 BLOCK DIAGRAM

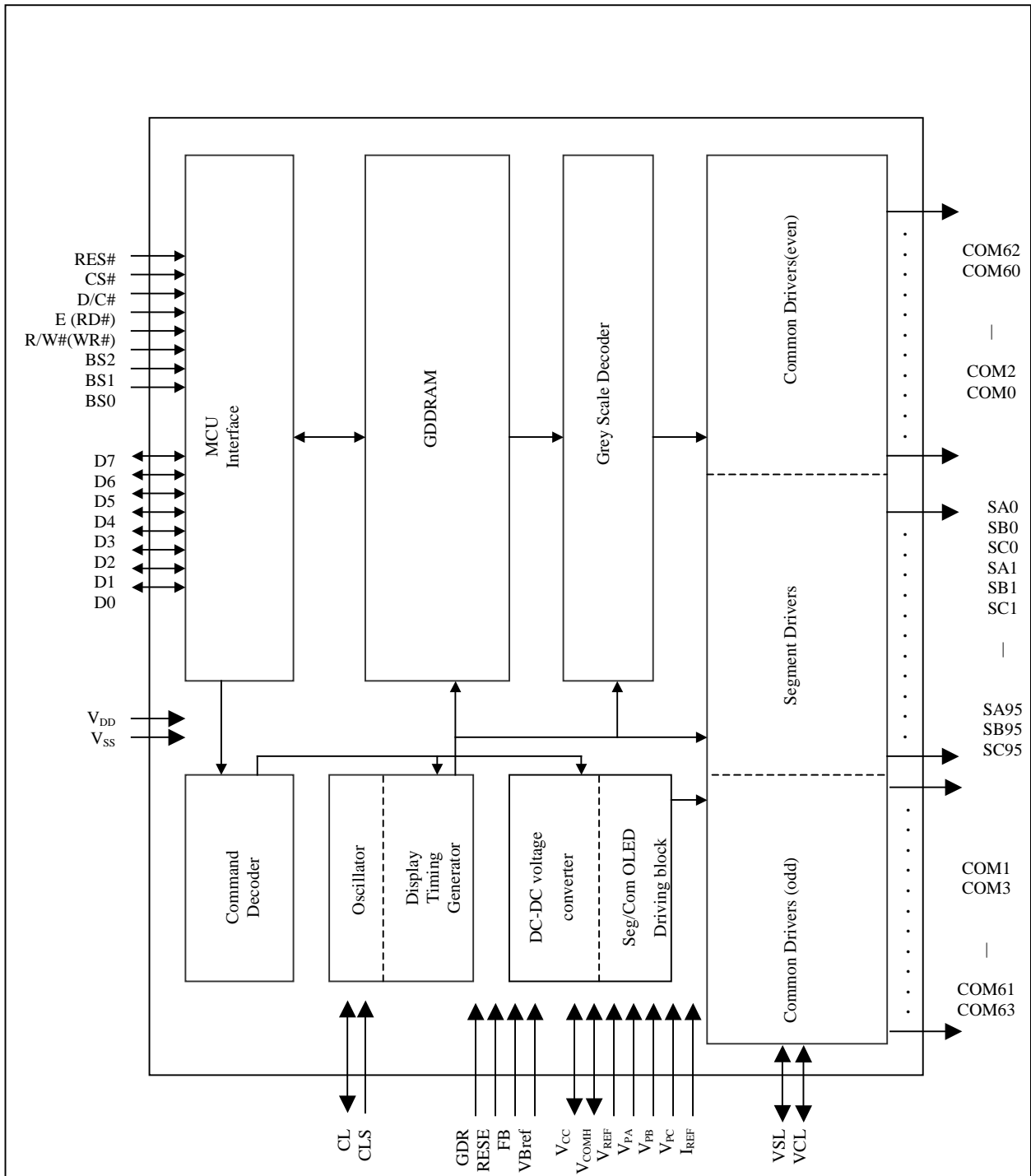
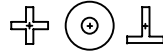
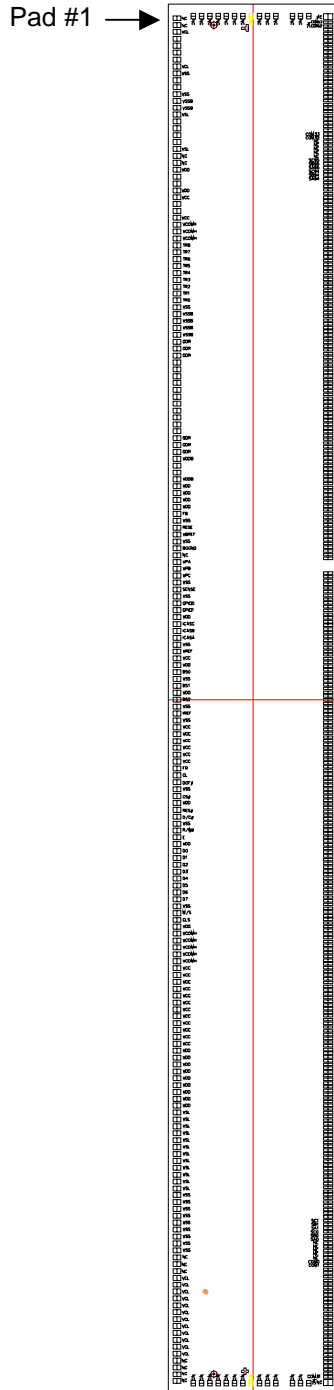


Figure 1 - Block Diagram

5 SSD1332Z GOLD BUMP DIE PAD ASSIGNMENT



+ represents the centre of the alignment mark

| | X-pos (μm) | Y-pos (μm) |
|--|-------------------------|-------------------------|
| | -7433.6 | -90.5 |
| | 7433.6 | -90.5 |
| | -7465.9 | -437.4 |
| | 7465.9 | -437.4 |

All alignment keys have size
75 μm x 75 μm

Die Size: 15.4mm x 1.9mm
Die Thickness: 457 +/- 25 μm
Min I/O pad pitch: 76.2 μm
Min SEG pad pitch: 41.2 μm
Min COM pad pitch: 41.2 μm
Bump Height: Nominal 15 μm

| Bump size / Pad # | X-Dimension | Y-Dimension |
|----------------------|----------------------|-----------------------|
| 1 - 199 | 54.000 μm | 84.000 μm |
| 200 ~ 213, 578 ~ 591 | 50.000 μm | 60.000 μm |
| 215 ~ 576 | 27.000 μm | 110.000 μm |
| 214, 577 | 68.200 μm | 110.000 μm |

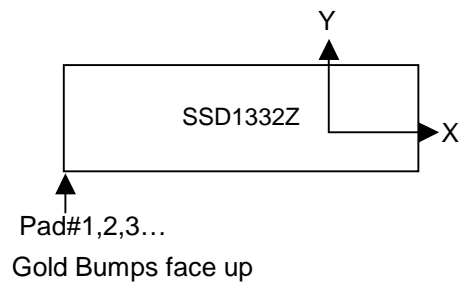
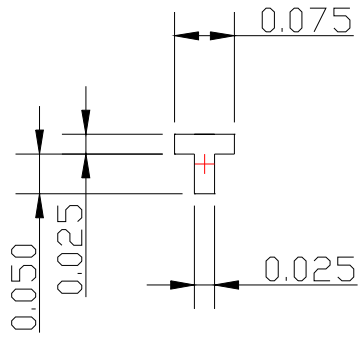
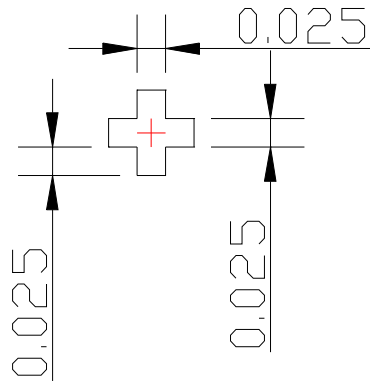


Figure 3 - SSD1332Z Alignment mark dimensions



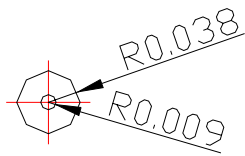
T shape

Detail T



+ shape

Detail +



Circle

Detail O

Scale: 10:1

Unit in um

6 PIN DESCRIPTION

BS0, BS1, BS2

These input pins are used to configure MCU interface selection by appropriate logic setting, which is described in the following table:

Table 3 – MCU Interface Selection Setting

| | 6800-parallel interface (8 bit) | 8080-parallel interface (8 bit) | Serial interface |
|-----|---------------------------------|---------------------------------|------------------|
| BS0 | 0 | 0 | 0 |
| BS1 | 0 | 1 | 0 |
| BS2 | 1 | 1 | 0 |

CS#

This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

RES#

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

D/C

This pin is Data/Command control pin. When the pin is pulled high, the data at D₇-D₀ is treated as display data. When the pin is pulled low, the data at D₇-D₀ will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

R/W(WR#)

This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.

When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected.

When serial interface is selected, this pin E(RD#) must be connected to VSS.

E (RD#)

This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.

When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected.

When serial interface is selected, this pin E(RD#) must be connected to VSS.

D₇-D₀

These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.

V_{DD}

Power Supply pin for logic operation of the driver. It must be connected to external source.

V_{SS}

Ground pin. It must be connected to external ground.

V_{CC}

This is the most positive voltage supply pin of the chip. It is supplied either by external high voltage source or internal booster

V_{REF}

This pin is the reference for OLED driving voltages like V_{PA}, V_{PB}, V_{PC} and V_{COMH}. The relation between V_{REF} and those driving voltages can be programmed and please refer to section "Command Table" for details. V_{REF} can be either supplied externally or connected to V_{CC}.

V_{PA}, V_{PB}, V_{PC}

These pins are the pre-charge driving voltages for OLED driving segment pins SA0-SA95, SB0-SB95 and SC0-SC95 respectively. They can be supplied externally or internally generated by VP circuit. When internal VP is used, V_{PA}, V_{PB}, V_{PC} pins should be left open.

I_{REF}

This pin is the segment output current reference pin. I_{SEG} is derived from I_{REF}

$$I_{SEG} = \text{Contrast} / 256 * I_{REF} * \text{scale factor},$$

in which the contrast is set by command and the scale factor = 1 ~ 16.

A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA. Please refer to section 6 "Current and Voltage Supply" for the formula of resistor value from I_{REF}.

V_{COMH}

This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When V_{COMH} is generated internally, a capacitor should be connected between this pin and V_{SS}.

V_{DDB}

This is the power supply pin for the internal buffer of the DC-DC voltage converter. $3.5V \geq V_{DDB} \geq V_{DD}$.

V_{SSB}

This is the GND pin for the internal buffer of the DC-DC voltage converter. It must be connected to V_{SS}.

GDR

This output pin drives the gate of the external NMOS of the booster circuit. Please refer to the DC-DC voltage converter section for connection details.

RESE

This pin connects to the source current pin of the external NMOS of the booster circuit. Please refer to the DC-DC voltage converter section for connection details.

V_{BREF}

This pin is the internal voltage reference of booster circuit. A stabilization capacitor, typically 1uF, should be connected between V_{BREF} and V_{SS}.

FB

This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level (Vcc). Please refer to the DC-DC voltage converter section for connection details.

COM0-COM63

These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off.

SA0-SA95, SB0-SB95, SC0-SC95

These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off.

The 288 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.

7 FUNCTIONAL BLOCK DESCRIPTIONS

Oscillator Circuit and Display Time Generator

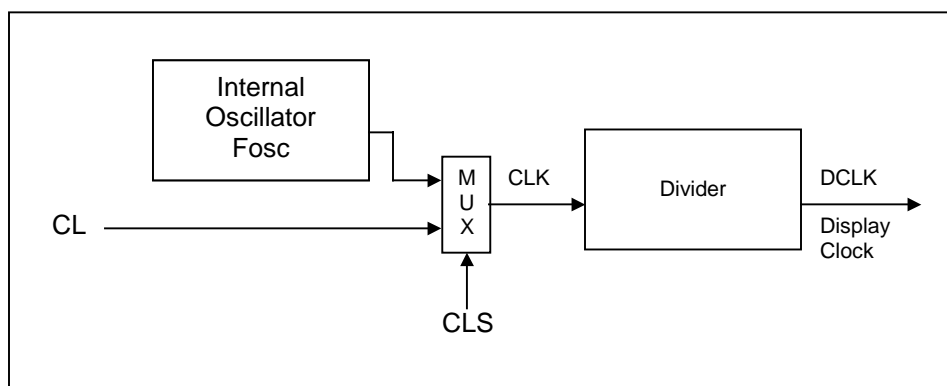


Figure 4 - Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is high, internal oscillator is selected. If CLS pin is low, external clock from CL pin will be used for CLK. The frequency of internal oscillator Fosc can be programmed by command B3h.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor can be programmed from 1 to 16 by command B3h.

Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 64 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Master contrast control register is set at 0FH
9. Individual contrast control registers of color A, B, and C are set at 80H

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is high, data is written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D₀-D₇ is interpreted as a Command and it will be decoded and be written to the corresponding command register.

Current and Voltage Supply

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} are most positive voltage supply. It can be supplied externally or from internal DC-DC converter.
- V_{DD} are external power supply for logic operation of the driver.
- V_{REF} is reference voltage, which is used to derive driving voltage for segments and commons like V_{PA} , V_{PB} , V_{PC} and V_{COMH} . Normally, V_{REF} is connected to V_{CC} . Please refer to the command table for the relationships of V_{REF} to the segments and commons voltages.
- I_{REF} is a reference current source for segment current drivers I_{SEG} . The relationship between reference current and segment current of a color is:

$$I_{SEG} = \text{Contrast} / 256 * I_{REF} * \text{scale factor}$$

in which the contrast (0~255) is set by Set Contrast command,
and the scale factor (1 ~ 16) is set by Master Current Control command.

For example, in order to achieve $I_{SEG} = 160\mu\text{A}$ at maximum contrast 255, I_{REF} is set to around $10\mu\text{A}$. This current value is obtained by connecting an appropriate resistor from I_{REF} pin to V_{SS} as shown in Figure 5.

Recommended range for $I_{ref} = 8 - 12\mu\text{A}$

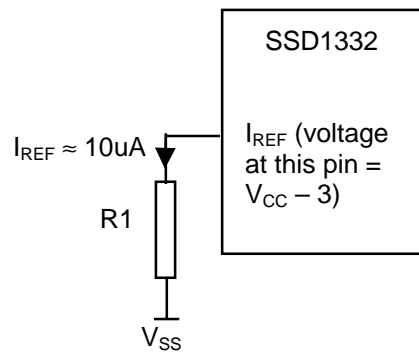


Figure 5 – I_{REF} Current Setting by Resistor Value

Since the voltage at I_{REF} pin is $V_{CC} - 3\text{V}$, the value of resistor $R1$ can be found as below.
 $R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} = (V_{CC} - 3) / 10\mu\text{A} \approx 910\text{k}\Omega$ for $V_{CC} = 12\text{V}$.

Segment Drivers/Common Drivers

Segment drivers consists of 288 (96 x 3 colors) current sources to drive OLED panel. The driving current can be adjusted from 0 to 200uA with 256 steps by contrast setting command. Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

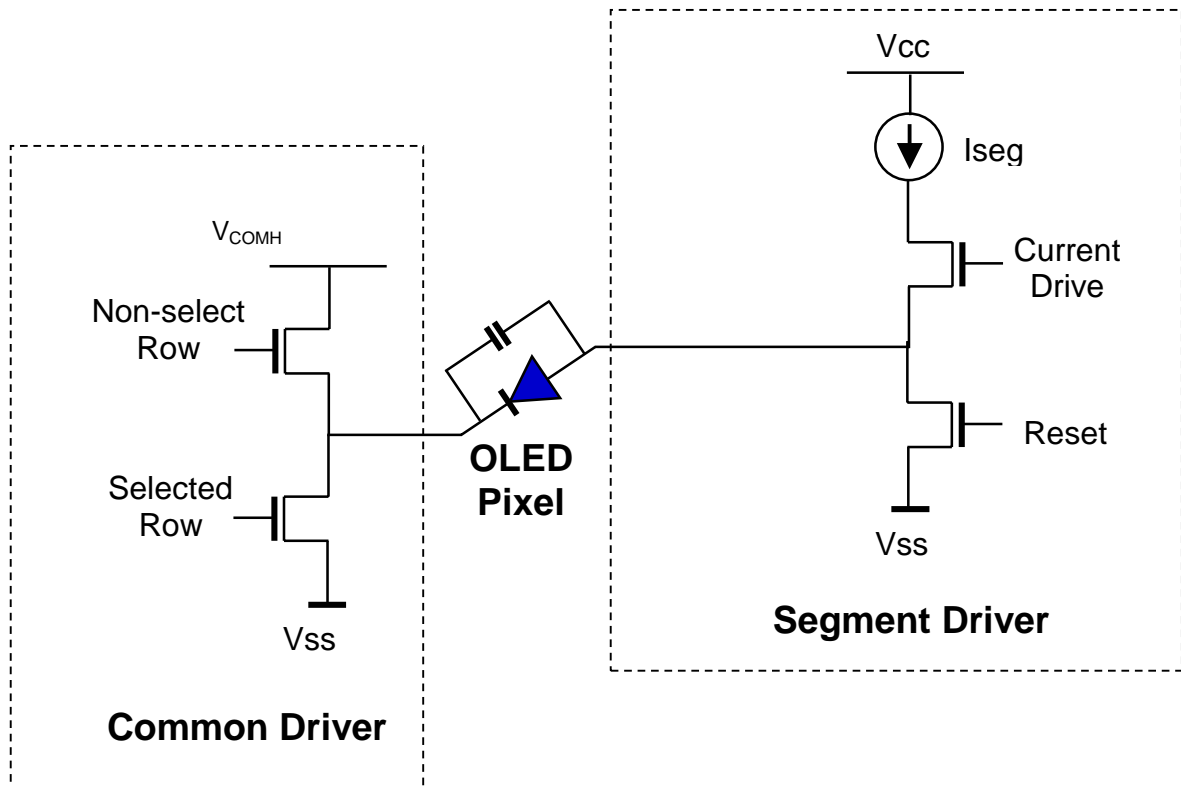


Figure 6 – Segment and Common Driver Block Diagram

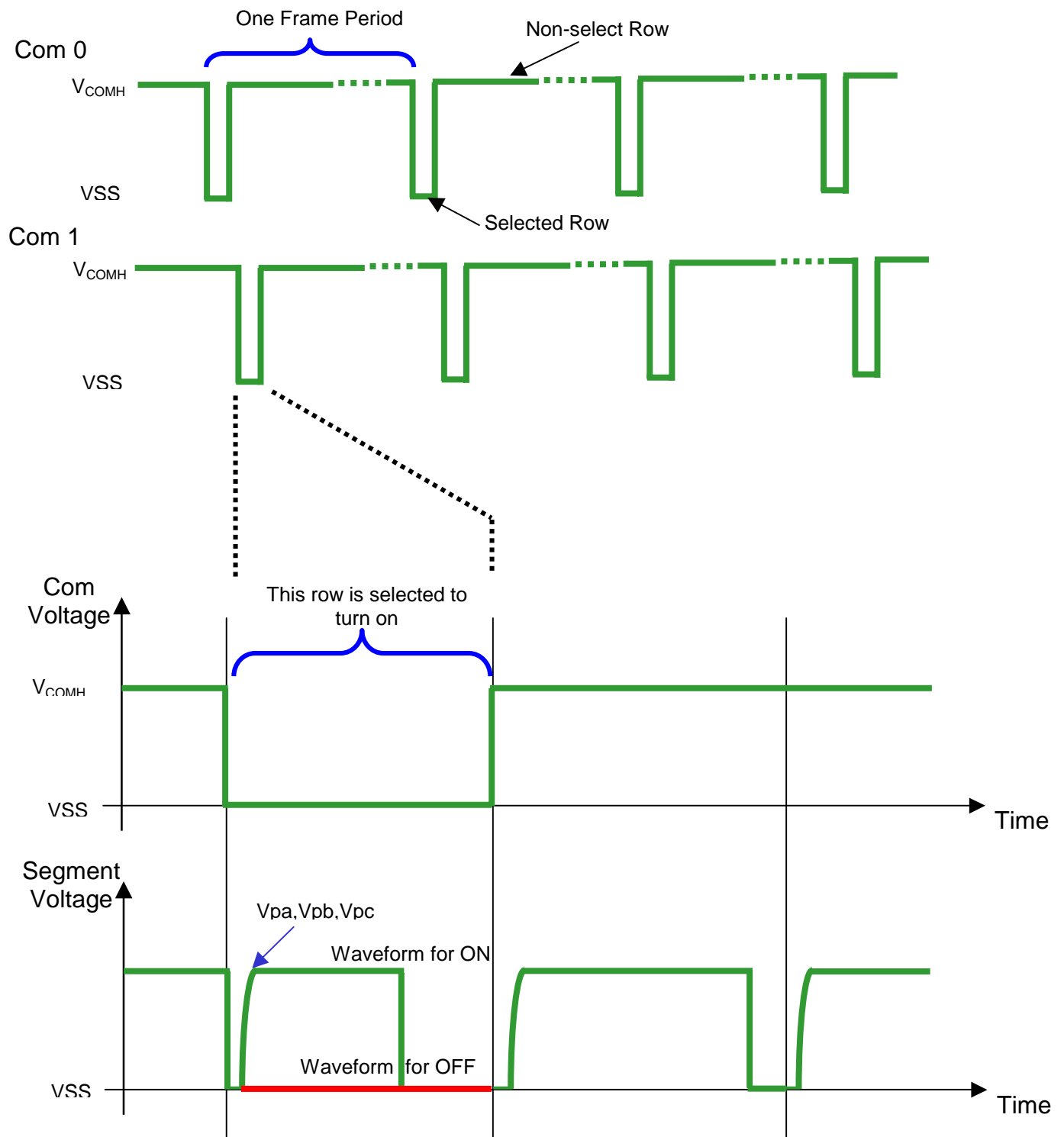


Figure 7 – Segment and Common Driver Signal Waveform

The commons are scanned sequentially one by one row. If the row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} .

In the scanned row, the pixels on the row will be turned on or off by sending the corresponding data signal to the segment pins. If the pixel is turned off, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned on.

There are three phases to driving a OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{SS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h from 1 to 16 DCLK. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, the pixel is charged up by the segment driver to the desired voltage levels V_{PA} , V_{PB} or V_{PC} for color A, B or C respectively. The period of phase 2 can be programmed by command B1h from 1 to 16 DCLK. An OLED panel with larger capacitance requires a longer period for charging up.

Last phase is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The wider pulse widths in the current drive stage results in brighter pixels and vice versa. This is shown in the following figure.

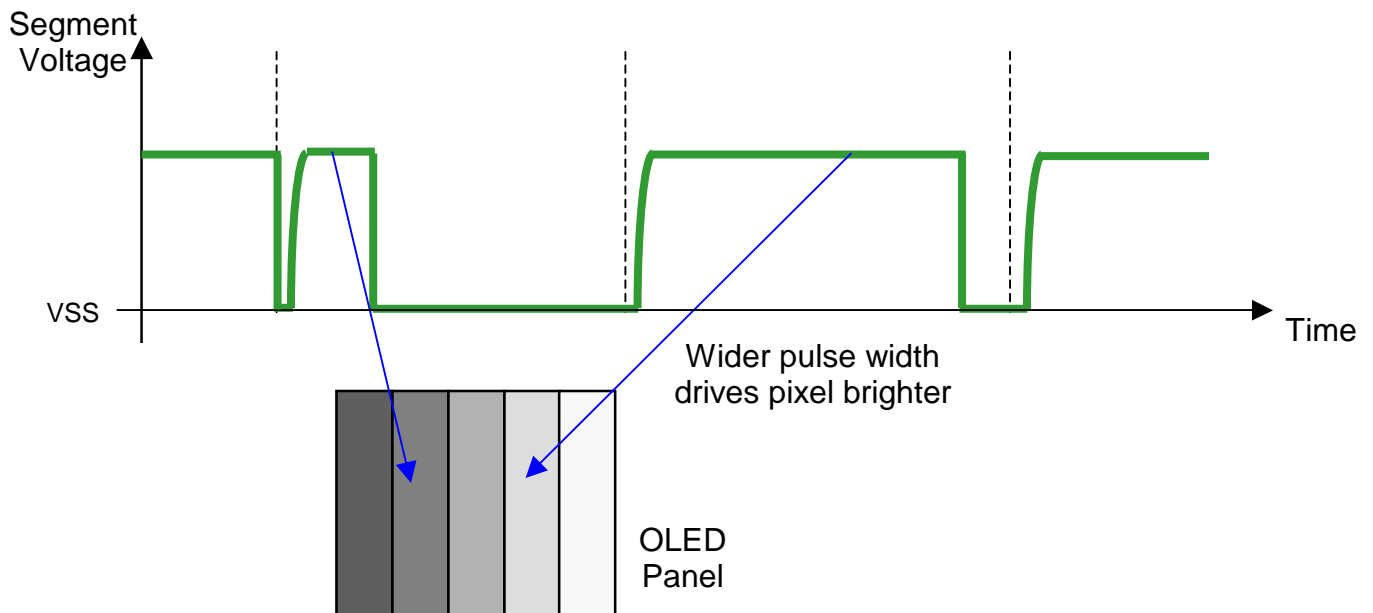


Figure 8 – Gray Scale Control by PWM in Segment

The pulse width in current drive stage to control brightness can be programmed through “Set Gray Scale Table” command. It is described in more detailed in “Command Descriptions” section.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0 - D_7), R/W(WR#), D/C, E (RD#) and CS#. R/W(WR#) High Input indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W(WR#) Low Input indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The E(RD#) input serves as data latch signal (clock) when high provided that CS# is low. Refer to Figure 27 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 9 below.

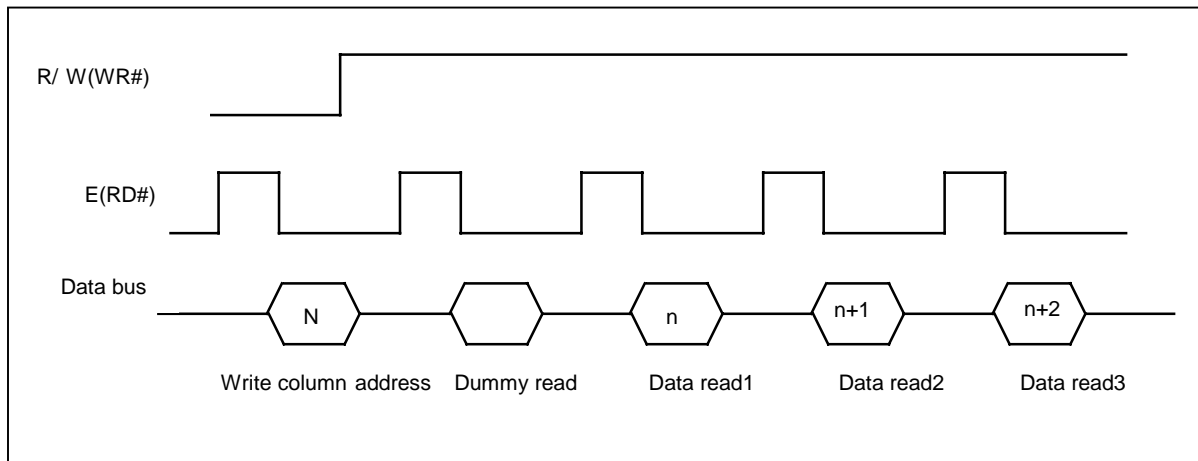


Figure 9 - Display data read back procedure - insertion of dummy read

MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0 - D_7), E (RD#), R/W(WR#), D/C and CS#. The E(RD#) input serves as data read latch signal (clock) when low, provided that CS# is low. Display data RAM or status register read is controlled by D/C#.

R/W(WR#) input serves as data write latch signal (clock) when low provided that CS# is low, or CS# input serves as data write latch signal at rising edge when R/W(WR#) is low. Display data RAM or command register write is controlled by D/C. Refer to Figure 28 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. D3 to D7, E and R/W pins can be connected to external ground.

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D_7, D_6, \dots, D_0 . D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The size of the RAM is 96 x 64 x 16bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Each pixel has 16-bit data. Three sub-pixels for color A, B and C have 6 bits, 5 bits and 6 bits respectively. The arrangement of data pixel in graphic display data RAM is shown below.

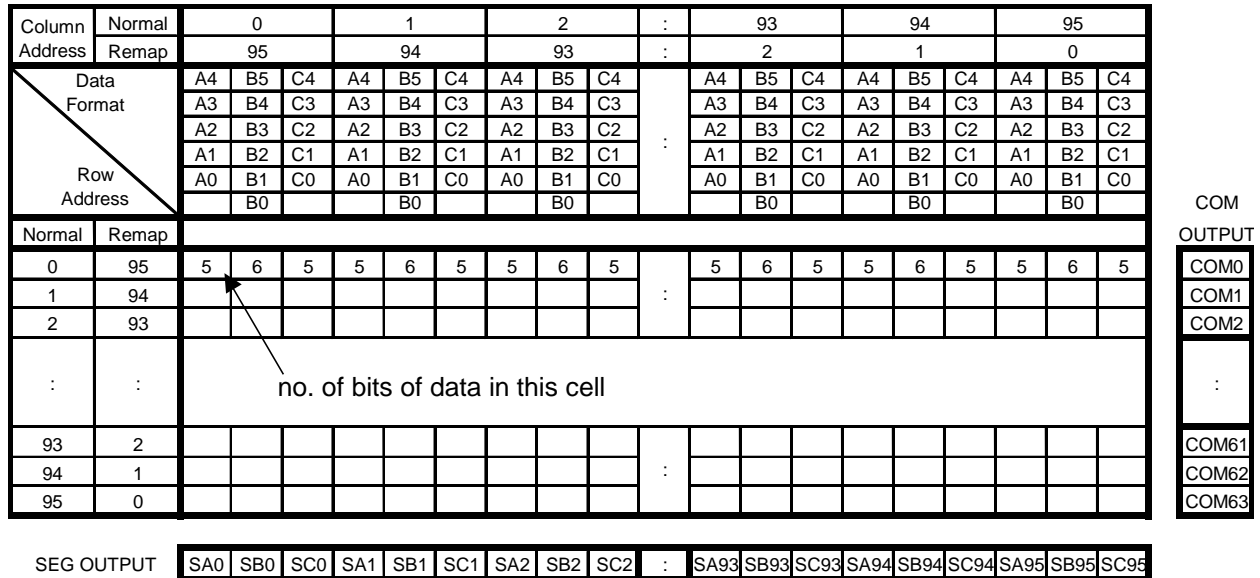


Figure 10 – 65k Color Depth Graphic Display Data RAM Structure

The sequence of sending one pixel of 16-bit data is divided into two 8-bit sessions as shown below.

| | | | | | | | | |
|----------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 1 st byte | C4 | C3 | C2 | C1 | C0 | B5 | B4 | B3 |
| 2 nd byte | B2 | B1 | B0 | A4 | A3 | A2 | A1 | A0 |

Figure 11 – 65k Color Depth Graphic Display Data Writing Sequence

In 256-color mode, each pixel is composed of 8-bit. Color A uses 2-bit while color B and color C each is represented by 3-bit. Although only 8 bits are required to represent one pixel, each pixel occupies 16-bit space inside graphic display data RAM with format as follows.

For 256-color mode, one pixel data is sent in a 8-bit session like below.

| | | | | | | | | |
|----------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 1 st byte | C2 | C1 | C0 | B2 | B1 | B0 | A1 | A0 |

Figure 11 – 256 Color Depth Graphic Display Data Writing Sequence

| Color C (3 bits) | RAM Content (5 bits) | Color B (3 bits) | RAM Content (6 bits) | Color A (2 bits) | RAM Content (5 bits) |
|---------------------|-----------------------------|---------------------|-----------------------------|---------------------|-----------------------------|
| 000 | 00000 | 000 | 000000 | 00 | 00000 |
| 001 | 00100 | 001 | 001000 | 01 | 01000 |
| 010 | 01000 | 010 | 010000 | 10 | 10100 |
| 011 | 01100 | 011 | 011000 | 11 | 11100 |
| 100 | 10010 | 100 | 100100 | | |
| 101 | 10110 | 101 | 101100 | | |
| 110 | 11010 | 110 | 110100 | | |
| 111 | 11110 | 111 | 111100 | | |

Figure 12 – 256 Color Depth Graphic Display Data RAM Structure for One Pixel

Gray Scale and Gray Scale Table

The gray scale display is produced by controlling the current pulse widths from the segment driver in the current drive phase. The gray scale table stores the corresponding pulse widths (PW0 ~ PW63) of the 64 gray scale levels (GS0~GS63). The wider the pulse width, the brighter the pixel will be. This single gray scale table supports all the three colors A, B and C. The pulse widths are entered by software commands.

As shown in figure 13, color B sub-pixel RAM data has 6 bits, represent the 64 gray scale levels from GS0 to GS63. color A and color C sub-pixel RAM data has only 5 bits, represent 32 gray scale levels from GS0, GS2, ..., GS62.

| Color A, C RAM data (5 bits) | Color B RAM data (6 bits) | Gray Scale |
|---------------------------------|------------------------------|------------|
| 0 | 0 | GS0 |
| - | 1 | GS 1 |
| 1 | 2 | GS 2 |
| - | 3 | GS 3 |
| 2 | 4 | GS 4 |
| : | : | : |
| : | : | : |
| : | : | : |
| 30 | 60 | GS 60 |
| - | 61 | GS 61 |
| 31 | 62 | GS 62 |
| - | 63 | GS 63 |

Figure 13 – Relation between graphic data RAM value and gray scale table entry for three colors in 65K color mode

The meaning of values inside data RAM with respect to the gray scale level is best to be illustrated in an example below.

| Gray Scale (Pulse Width) | Value/DCLKs |
|--------------------------|-------------|
| PW0 | 0 |
| PW1 | 2 |
| PW2 | 5 |
| : | : |
| PW62 | 120 |
| PW63 | 125 |

Gray Scale Table

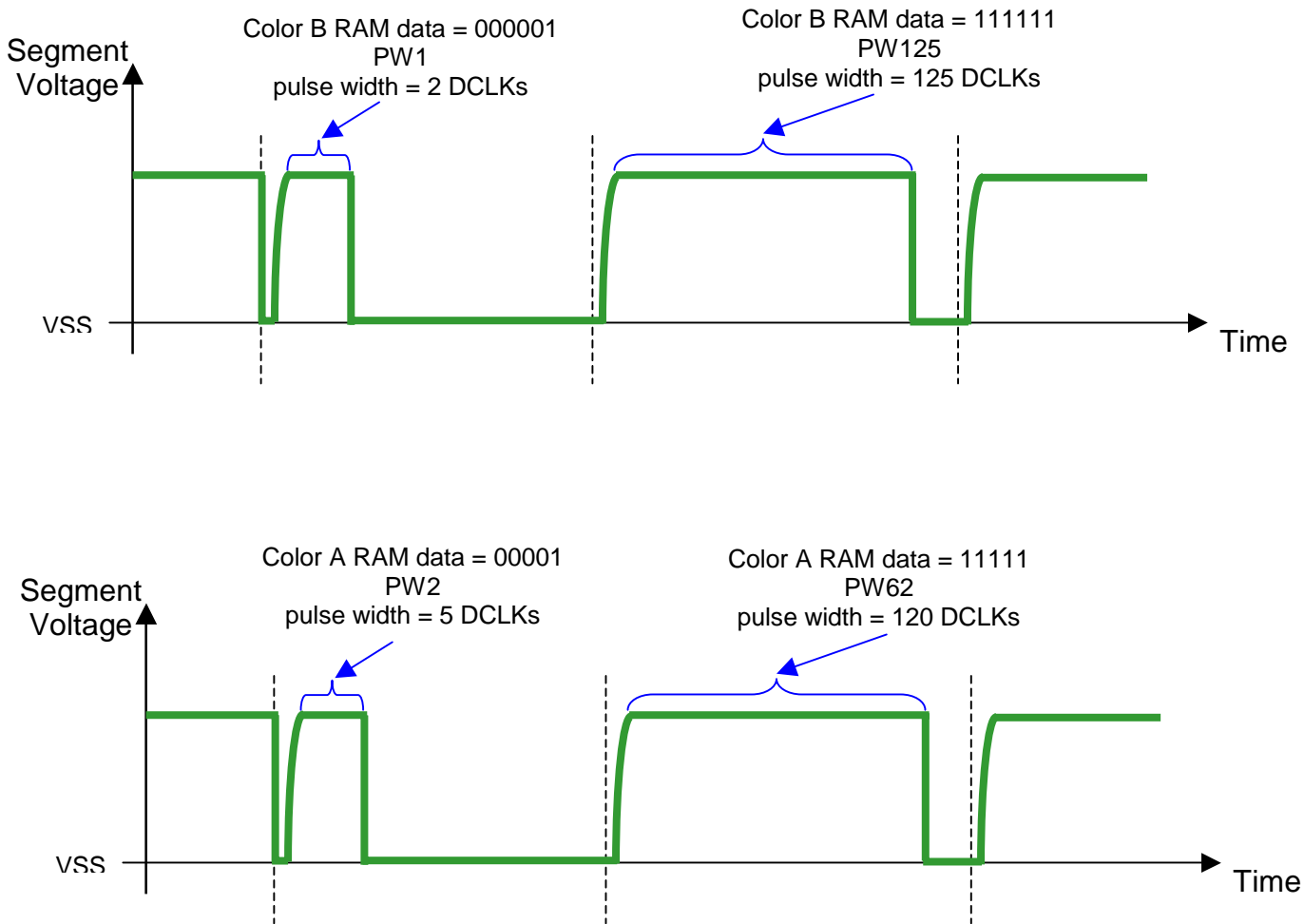


Figure 14 – illustration of relation between graphic display RAM value and gray scale control

DC-DC Voltage Converter

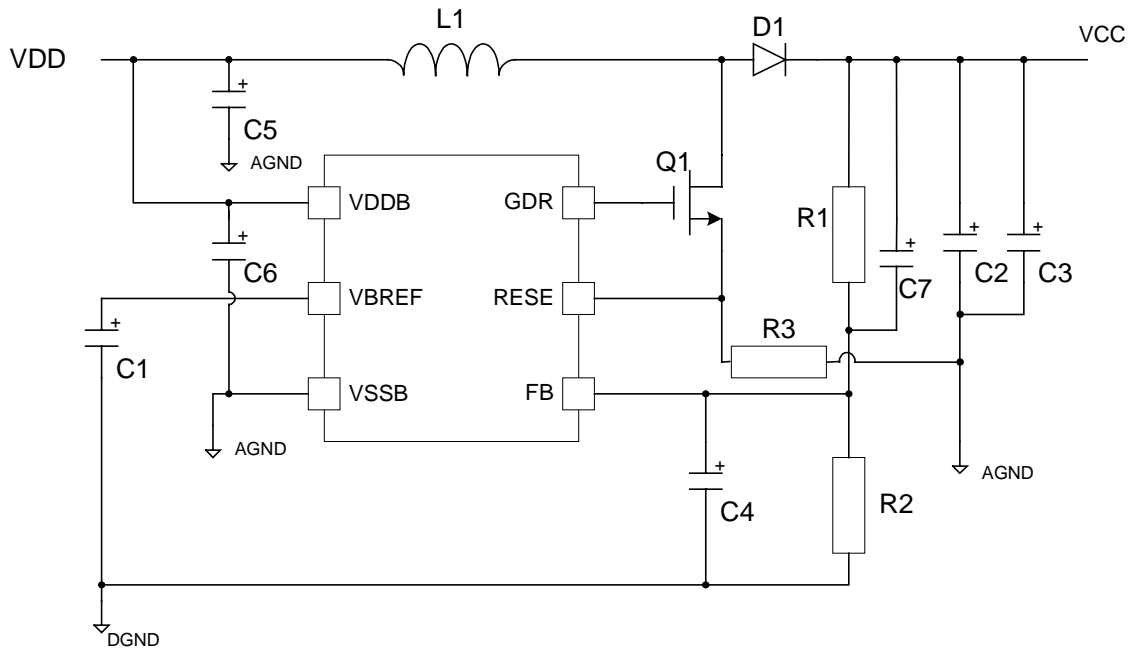


Figure 15 – DC-DC Converter Application Circuit Diagram

It is a switching voltage generator circuit, designed for handheld applications. In SSD1332, internal DC-DC voltage converter accompanying with an external application circuit (shown in Figure 15) can generate a high voltage supply V_{CC} from a low voltage supply input V_{DD} . V_{CC} is the voltage supply to the OLED driver block. The application circuit above is an example for the input voltage of 3V V_{DD} to generate V_{CC} of 12V @20mA ~ 30mA application.

*ALL PATHS TO AGND SHOULD BE CONNECTED AS SHORT AS POSSIBLE

Passive components selection:

Table 4 – Components Selection for DC-DC Converter

| Components | Typical Value | Remark |
|------------|----------------------------|--|
| L1 | Inductor, 22 μ H | 2A |
| D1 | Schottky diode | 2A, 25V e.g. 1N5822 |
| Q1 | MOSFET | N-FET with low $R_{DS(on)}$ and low V_{th} voltage. e.g. MGSF1N02LT1 [ON SEMICONDUCTOR] |
| R1, R2 | Resistor | 1%, 1/10W |
| R3 | Resistor, 1.2 Ω | 1%, 1/2W |
| C1 | Capacitor, 1 μ F | 16V |
| C2 | Capacitor, 22 μ F | Low ESR, 25V |
| C3 | Capacitor, 1 μ F | 16V |
| C4 | Capacitor, 10nF | 16V |
| C5 | Capacitor, 1 ~ 10 μ F | 16V |
| C6 | Capacitor, 0.1 ~ 1 μ F | 16V |
| C7 | Capacitor, 15nF | 16V |

The VCC output voltage level can be adjusted by R1 and R2, the reference formula is:

$$V_{CC} = 1.2 \times (R1+R2) / R2$$

8 COMMAND TABLE

Table 5 – Configuration Command Table

(To write commands to command registers, the MCU interface pins are set as: D/C = 0, R/W(WR#) = 0, E (RD#)=1)

| D/C | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|-------------|------------------------|---------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|--|--|
| 0 0 0 | 15 A[6:0] B[6:0] | 0 * * | 0 A ₆ B ₆ | 0 A ₅ B ₅ | 1 A ₄ B ₄ | 0 A ₃ B ₃ | 1 A ₂ B ₂ | 0 A ₁ B ₁ | 1 A ₀ B ₀ | Set Column Address | A[6:0] sets the column start address from 0-95, POR=00d. B[6:0] sets the column end address from 0-95 POR=95d. |
| 0 0 0 | 75 A[5:0] B[5:0] | 0 * * | 1 * * | 1 A ₅ B ₅ | 1 A ₄ B ₄ | 0 A ₃ B ₃ | 1 A ₂ B ₂ | 0 A ₁ B ₁ | 1 A ₀ B ₀ | Set Row Address | A[5:0] sets the row start address from 0-63, POR=00d. B[5:0] sets the row end address from 0-63, POR=63d. |
| 0 0 | 81 A[7:0] | 1 A ₇ | 0 A ₆ | 0 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Contrast for Color A (Segment Pins :SA0 – SA95) | Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H |
| 0 0 | 82 A[7:0] | 1 A ₇ | 0 A ₆ | 0 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 0 A ₀ | Set Contrast for Color B (Segment Pins :SB0 – SB95) | Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H |
| 0 0 | 83 A[7:0] | 1 A ₇ | 0 A ₆ | 0 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 1 A ₀ | Set Contrast for Color C (Segment Pins :SC0 – SC95) | Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H |
| 0 0 | 87 A[3:0] | 1 * | 0 * | 0 * | 0 * | 0 A ₃ | 1 A ₂ | 1 A ₁ | 1 A ₀ | Master Current Control | Set A[3:0] from 0000, 0001... to 1111 to adjust the master current attenuation factor from 1/16, 2/16... to 16/16. POR =1111b, for no attenuation. |

| | | | | | | | | | | | |
|--------|--------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------------------|--|
| 0 0 | A0 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 0 A ₄ | 0 * | 0 * | 0 A ₁ | 0 A ₀ | Set Re-map & Data Format | <p>A[0]=0, Horizontal address increment (POR) A[0]=1, Vertical address increment</p> <p>A[1]=0, Column address 0 is mapped to SEG0 (POR) A[1]=1, Column address 95 is mapped to SEG0</p> <p>A[4]=0, Scan from COM 0 to COM [N-1] A[4]=1, Scan from COM [N-1] to COM0. Where N is the Multiplex ratio.</p> <p>A[5]=0, Disable COM Split Odd Even (POR) A[5]=1, Enable COM Split Odd Even</p> <p>A[7:6]=00; 256 color format = 01; 65k color format(POR)</p> |
| 0 0 | A1 A[5:0] | 1 * | 0 * | 1 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Display Start Line | <p>Set display RAM display start line register from 0-63. Display start line register is reset to 00H after POR.</p> |
| 0 0 | A2 A[5:0] | 1 * | 0 * | 1 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 0 A ₀ | Set Display Offset | <p>Set vertical scroll by COM from 0-63. The value is reset to 00H after POR.</p> |
| 0 | A4~A7 | 1 | 0 | 1 | 0 | 0 | 1 | X ₁ | X ₀ | Set Display Mode | <p>A4h=Normal Display (POR) A5h=Entire Display On, all pixels turn on at GS level 63 A6h=Entire Display Off, all pixels turn off A7h=Inverse Display</p> |
| 0 0 | A8 A[5:0] | 1 * | 0 * | 1 A ₅ | 0 A ₄ | 1 A ₃ | 0 A ₂ | 0 A ₁ | 0 A ₀ | Set Multiplex Ratio | <p>The next command determines multiplex ratio N from 16MUX-64MUX, POR=63d (64MUX) A[5:0]=0-14d (invalid entry)</p> |
| 0 0 | AD A[7:0] | 1 1 | 0 0 | 1 0 | 0 0 | 1 1 | 1 A ₂ | 0 A ₁ | 1 A ₀ | Set Master Configuration | <p>A[0]=0, Select external VCC supply at Display ON A[0]=1, Select internal booster at Display ON (POR)</p> <p>A[1]=0, Select external VCOMH voltage supply at Display ON A[1]=1, Select internal VCOMH regulator at Display ON (POR)</p> <p>A[2]=0, Select External VP voltage supply A[2]=1, Select Internal VP (POR)</p> |
| 0 | AE~AF | 1 | 0 | 1 | 0 | X ₃ | 1 | 1 | 1 | Set Display On/Off | <p>A Eh=Display off (POR) A Fh=Display on</p> |
| 0 0 | B0 A[7:0] | 1 0 | 0 0 | 1 0 | 1 A ₄ | 0 0 | 0 0 | 0 A ₁ | 0 0 | Set Power Save | <p>A[7:0]=00 (POR) A[7:0]=12, power saving mode</p> |
| 0 0 | B1 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Phase 1 and 2 period adjustment | <p>A[3:0] Phase 1 period in 1~16 DCLK clocks [POR=4h] A[7:4] Phase 2 period in 1~16 DCLK clocks [POR=7h]</p> |

| | | | | | | | | | | | |
|---|---|---------------------|---------------------|---------------------|---------------------|---------------------|----------------------------------|----------------------------------|----------------------------------|--|---|
| 0 0 | B3 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 1 A ₀ | Display Clock Divider / Oscillator Frequency | A[3:0] [DIVIDER, POR=0] DCLK is generated from CLK divided by DIVIDER +1 (i.e., 1 to 16) A[7:4] Fosc frequency, POR=D0H Frequency increases as level increases |
| 0 0 0 0 0 0 0 0 0 0 0 | B8 A[7:0]-- PW1 B[7:0]-- PW3 C[7:0]-- PW5 : : : : AE[7:0]-- PW61 AF[7:0]-- PW63 | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 1 A ₃ | 0 A ₂ | 0 A ₁ | 0 A ₀ | Set Gray Scale Table | The next 32 bytes of command set the current drive pulse width of gray scale level GS1, GS3, GS5 ...GS63 as below: A[7:0]=PW1, POR=1, it equals 1 DCLK clock B[7:0]=PW3, POR=5, it equals 3 DCLK clocks C[7:0]=PW5, POR= 9 : : : : AE[7:0]=PW61, POR=121 AF[7:0]=PW63, POR=125, it equals 125 DCLK clocks Note: GS0 has no pre-charge and current drive stages. For GS2 GS4...GS62, they are derived by driver itself with: PW _n = (PW _{n-1} +PW _{n+1})/2 Max pulse width is 125 |
| 0 | B9 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | | Enable Linear Gray Scale Table |
| 0 0 | BB ~ BD A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 1 A ₃ | X ₂ A ₂ | X ₁ A ₁ | X ₀ A ₀ | V _{PA} , V _{PB} , V _{PC} level setting for Color A,B,C | 011b for Color A, 100b for Color B, 101b for Color C A[7:0] 00000000 0.43*Vref 00111111 0.83*Vref 01111111 1.0*Vref 1xxxxxxx connects to VCOMH (POR) |
| 0 0 | BE A[6:0] | 1 * | 0 A ₆ | 1 A ₅ | 1 A ₄ | 1 A ₃ | 1 A ₂ | 1 A ₁ | 0 A ₀ | Set VCOMH | A[6:0] 0000000 0.43*Vref 0111111 0.83*Vref (POR) |
| 0 | E3 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | NOP | Command for No Operation |

Table 6 – Graphic Acceleration Command Set Table

(To write commands to command registers, the MCU interface pins are set as: D/C = 0, R/W(WR#)=0, E (RD#)=1)

| D/C | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|-----|--------|----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------------|---|
| 0 | 21 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Draw Line | A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End E[5:1] : Color C of the line F[5:0] : Color B of the line G[5:1] : Color A of the line |
| 0 | A[6:0] | * | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | |
| 0 | B[5:0] | * | * | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | |
| 0 | C[6:0] | * | C ₆ | C ₅ | C ₄ | C ₃ | C ₂ | C ₁ | C ₀ | | |
| 0 | D[5:0] | * | * | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | | |
| 0 | E[5:1] | * | * | E ₅ | E ₄ | E ₃ | E ₂ | E ₁ | * | | |
| 0 | F[5:0] | * | * | F ₅ | F ₄ | F ₃ | F ₂ | F ₁ | F ₀ | | |
| 0 | G[5:1] | * | * | G ₅ | G ₄ | G ₃ | G ₂ | G ₁ | * | | |
| 0 | 22 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | | Drawing Rectangle |
| 0 | A[6:0] | * | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | |
| 0 | B[5:0] | * | * | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | |
| 0 | C[6:0] | * | C ₆ | C ₅ | C ₄ | C ₃ | C ₂ | C ₁ | C ₀ | | |
| 0 | D[5:0] | * | * | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | | |
| 0 | E[5:1] | * | * | E ₅ | E ₄ | E ₃ | E ₂ | E ₁ | * | | |
| 0 | F[5:0] | * | * | F ₅ | F ₄ | F ₃ | F ₂ | F ₁ | F ₀ | | |
| 0 | G[5:1] | * | * | G ₅ | G ₄ | G ₃ | G ₂ | G ₁ | * | | |
| 0 | H[5:1] | * | * | H ₅ | H ₄ | H ₃ | H ₂ | H ₁ | * | | |
| 0 | I[5:0] | * | * | I ₅ | I ₄ | I ₃ | I ₂ | I ₁ | I ₀ | | |
| 0 | J[5:1] | * | * | J ₅ | J ₄ | J ₃ | J ₂ | J ₁ | * | | |
| 0 | 23 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | Copy | A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End E[6:0] : Column Address of New Start F[5:0] : Row Address of New Start |
| 0 | A[6:0] | * | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | |
| 0 | B[5:0] | * | * | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | |
| 0 | C[6:0] | * | C ₆ | C ₅ | C ₄ | C ₃ | C ₂ | C ₁ | C ₀ | | |
| 0 | D[5:0] | * | * | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | | |
| 0 | E[6:0] | * | E ₆ | E ₅ | E ₄ | E ₃ | E ₂ | E ₁ | E ₀ | | |
| 0 | F[5:0] | * | * | F ₅ | F ₄ | F ₃ | F ₂ | F ₁ | F ₀ | | |
| 0 | 24 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | Dim Window | A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End The effect of dim window: GS15~GS0 no change GS19~GS16 become GS4 GS23~GS20 become GS5 ... GS63~GS60 become GS15 |
| 0 | A[6:0] | * | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | |
| 0 | B[5:0] | * | * | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | |
| 0 | C[6:0] | * | C ₆ | C ₅ | C ₄ | C ₃ | C ₂ | C ₁ | C ₀ | | |
| 0 | D[5:0] | * | * | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | | |
| 0 | 25 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | Clear Window | A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End |
| 0 | A[6:0] | * | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | |
| 0 | B[5:0] | * | * | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | |
| 0 | C[6:0] | * | C ₆ | C ₅ | C ₄ | C ₃ | C ₂ | C ₁ | C ₀ | | |
| 0 | D[5:0] | * | * | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | | |

| D/C | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|-----|--------|----|----|----|----------------|----|----|----|----------------|-----------------------|--|
| 0 | 26 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | Fill Enable / Disable | A0 0 : Disable Fill for Draw Rectangle Command (POR) 1 : Enable Fill for Draw Rectangle Command |
| 0 | A[4:0] | * | * | * | A ₄ | 0 | 0 | 0 | A ₀ | | A[3:1] 000 : Reserved values A4 0 : Disable reverse copy (POR) 1 : Enable reverse during copy command. |

Table 7 - Read Command Table

(D/C=0, R/W (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

| Bit Pattern | Command | Description |
|---|------------------------|--|
| D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀ | Status Register Read * | D ₇ : "1" for Command lock D ₆ : "1" for display OFF / "0" for display ON D ₅ : Reserve D ₄ : Reserve D ₃ : Reserve D ₂ : Reserve D ₁ : Reserve D ₀ : Reserve |

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

Data Read / Write

To read data from the GDDRAM, input HIGH to R/W (WR#) pin and D/C pin for 6800-series parallel mode, LOW to E (RD#) pin and HIGH to D/C pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read. See Figure 5 in Functional Block Description.

To write data to the GDDRAM, input LOW to R/W (WR#) pin and HIGH to D/C pin for 6800-series parallel mode AND 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

Table 8 - Address increment table (Automatic)

| D/C | R/W (WR#) | Comment | Address Increment |
|-----|-----------|---------------|-------------------|
| 0 | 0 | Write Command | No |
| 0 | 1 | Read Status | No |
| 1 | 0 | Write Data | Yes |
| 1 | 1 | Read Data | Yes |

9 COMMAND DESCRIPTIONS

Set Column Address (15h)

This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address.

Set Row Address (75h)

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

For example, column start address is set to 2 and column end address is set to 93, row start address is set to 1 and row end address is set to 62. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 93 and from row 1 to row 62 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation. Whenever the column address pointer finishes accessing the end column 93, it is reset back to column 2 and row address is automatically increased by 1. While the end row 62 and end column 93 RAM location is accessed, the row address is reset back to 1. The diagram below shows the way of column and row address pointer movement for this example.

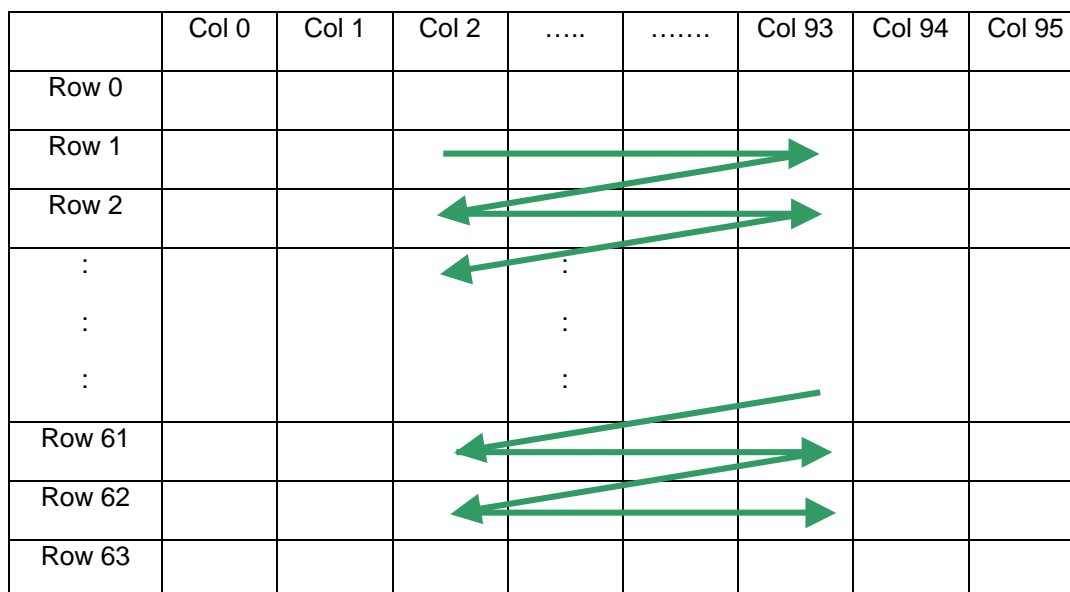


Figure 16 – Example of Column and Row Address Pointer Movement

Set Contrast for Color A, B, C (81h, 82h, 83h)

This command is to set Contrast Setting of each color A, B and C. The chip has three contrast control circuits for color A, B and C. Each contrast circuit has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter of the color. This relation is shown in Figure 17. In many situations, the output brightness of color A, B and C pixels are different under the same segment current condition. The contrasts of color A, B and C are set such that the brightness of each color are the same on the OLED panel

Master Current Control (87h)

This command is to control the segment output current by a scale factor. This factor is common to color A, B and C. The chip has 16 master control steps. The factor is ranged from 1 [0000] to 16 [1111]. POR is 16 [1111]. The smaller the master current value, the dimmer the OLED panel display is set. For example, if original segment output current of a color is 160uA at scale factor = 16, setting scale factor to 8 to reduce the current to 80uA. Please see Figure 17.

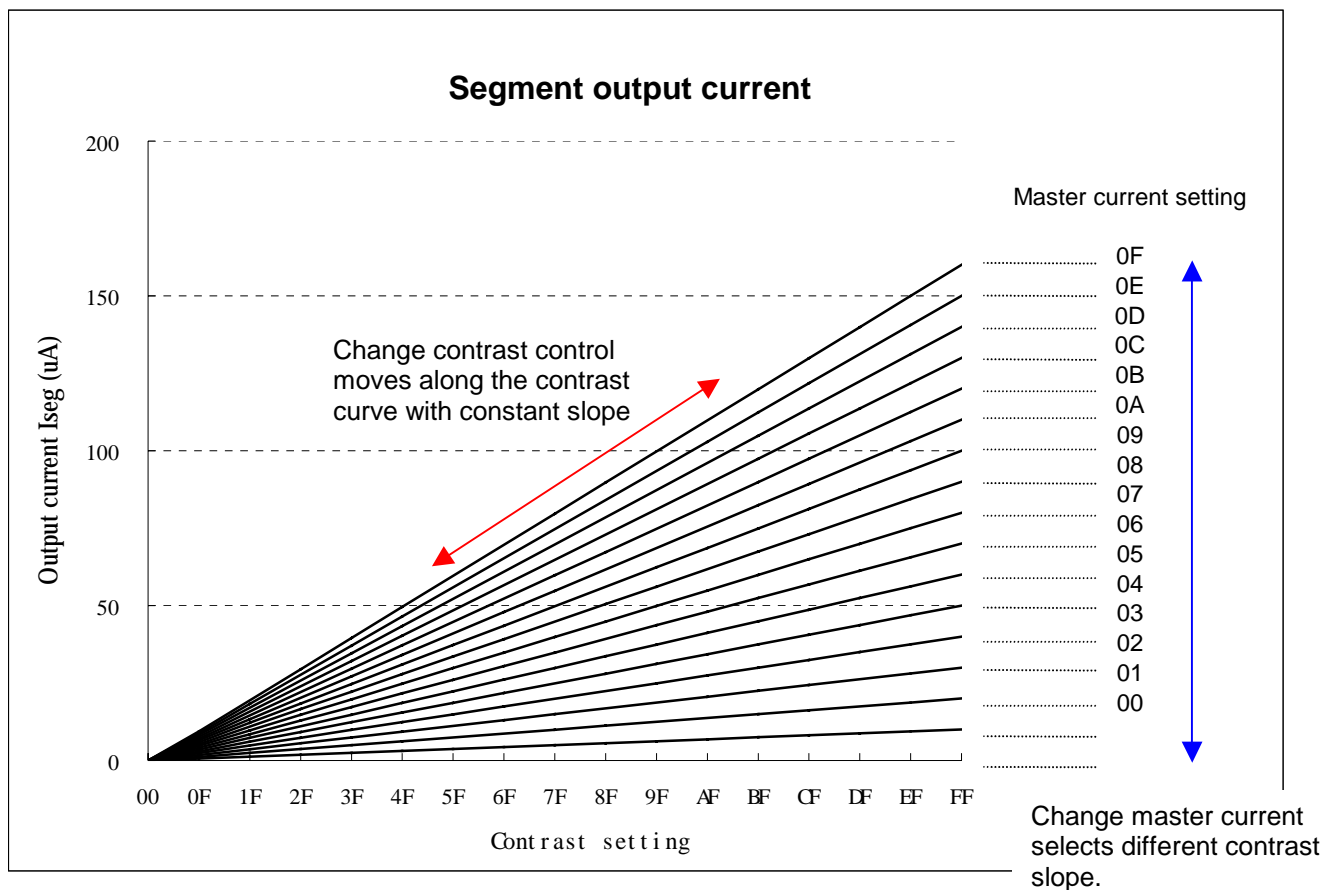


Figure 17 – Segment Output Current for Different Contrast Control and Master Current Setting

Set Re-map & Data Format (A0h)

This command has multiple configurations and each bit setting is described as follows.

- Address increment mode (A[0])
When it is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 18.

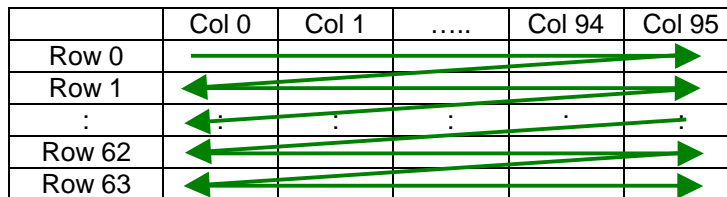


Figure 18 – Address Pointer Movement of Horizontal Address Increment Mode

When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 19.

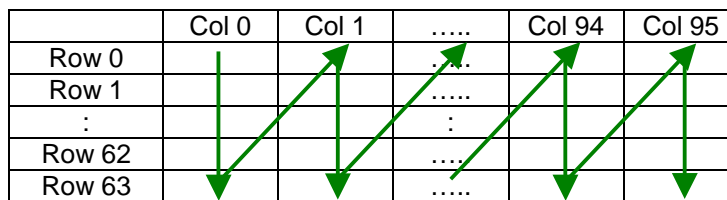


Figure 19 – Address Pointer Movement of Vertical Address Increment Mode

- Column Address Mapping (A[1])
This command bit is made for flexible layout of segment signals in OLED module with segment arranged from left to right or vice versa.
- COM Remap (A[4])
This bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa.
- Odd even split of COM pins (A[5])
This bit can set the odd even arrangement of COM pins.
A[5] = 0: Disable COM split odd even, pin assignment of common is in sequential as
COM63 COM62 COM 33 COM32..SC95..SA0..COM0 COM1.... COM30 COM31
A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
COM63 COM61.... COM3 COM1..SC95..SA0..COM0 COM2.... COM60 COM62
- Display color mode (A[7:6])
Select either 65k or 256 color mode. The display RAM data format in different mode is described in section “Graphic Display Data RAM (GDDRAM)”.

Set Display Start Line (A1h)

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

| | 64 | 64 | 62 | 62 | Mux ratio |
|---------|-------|-------|-------|-------|--------------------|
| COM Pin | 0 | 4 | 0 | 4 | Display start line |
| COM0 | Row0 | Row4 | Row0 | Row4 | |
| COM1 | Row1 | Row5 | Row1 | Row5 | |
| COM2 | Row2 | Row6 | Row2 | Row6 | |
| COM3 | Row3 | Row7 | Row3 | Row7 | |
| : | : | : | : | : | |
| : | : | : | : | : | |
| COM57 | Row57 | Row61 | Row57 | Row61 | |
| COM58 | Row58 | Row62 | Row58 | Row62 | |
| COM59 | Row59 | Row63 | Row59 | Row63 | |
| COM60 | Row60 | Row0 | Row60 | Row0 | |
| COM61 | Row61 | Row1 | Row61 | Row1 | |
| COM62 | Row62 | Row2 | - | - | |
| COM63 | Row63 | Row3 | - | - | |

Figure 20 – Example of Set Display Start Line with no Remap

Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-63. For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second command should be given by 0010000. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

| | 64 | 64 | 62 | 62 | Mux ratio |
|---------|-------|-------|-------|-------|----------------|
| COM Pin | 0 | 4 | 0 | 4 | Display offset |
| COM0 | Row0 | Row4 | Row0 | Row4 | |
| COM1 | Row1 | Row5 | Row1 | Row5 | |
| COM2 | Row2 | Row6 | Row2 | Row6 | |
| COM3 | Row3 | Row7 | Row3 | Row7 | |
| : | : | : | : | : | |
| : | : | : | : | : | |
| COM57 | Row57 | Row61 | Row57 | Row61 | |
| COM58 | Row58 | Row62 | Row58 | - | |
| COM59 | Row59 | Row63 | Row59 | - | |
| COM60 | Row60 | Row0 | Row60 | Row0 | |
| COM61 | Row61 | Row1 | Row61 | Row1 | |
| COM62 | Row62 | Row2 | - | Row2 | |
| COM63 | Row63 | Row3 | - | Row3 | |

Figure 21 – Example of Set Display Offset with no Remap

Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display On, Entire Display Off and Inverse Display.

- Set Entire Display On (A5h)
Forces the entire display to be at "GS63" regardless of the contents of the display data RAM.
- Set Entire Display Off (A6h)
Forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM.
- Inverse Display (A7h)
The gray level of display data are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62",
- Normal Display (A4h)
Reset the above effect and turn the data to ON at the corresponding gray level.

Set Multiplex Ratio (A8h)

This command switches default 1:64 multiplex mode to any multiplex mode from 16 to 64. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h.

Set Master Configuration (ADh)

This command contains multiple bits to control several functionalities of the driver.

- Select DC-DC converter (A[0])
0 = Disable selection of DC-DC converter and VCC is supplied externally.
1 (POR) = Enable selection of DC-DC converter to supply high voltage to VCC. The output voltage of the converter is set by values of external resistors. Please refer to section "DC-DC Voltage Converter" for details.
- Select V_{COMH} supply (A[1])
0 = Select external V_{COMH} voltage from V_{COMH} pin for the common waveform high voltage level supply. It is recommended to set the voltage of V_{COMH} such that the OLED pixel diode is not turned on (prefer in reverse bias state) when the segment pin is either driven to V_{PA} , V_{PB} or V_{PC} level.
1 = Select internal V_{COMH} voltage generated by regulator from V_{REF} . The level of V_{COMH} can be programmed by command BEh.
- Select pre-charge voltage supply (A[2])
0 = Select pre-charge voltage sources from external pins V_{PA} , V_{PB} , V_{PC} for color A, B and C respectively.
1 = Select pre-charge voltage supply internally. The level of V_{PA} , V_{PB} , V_{PC} can be set by command BBh, BCh and BDh for color A, B and C respectively.

Set Display On/Off (AEh/AFh)

These single byte commands are used to turn the OLED panel display on or off. When the display is on, the selected circuits by Set Master Configuration command will be turned on. When the display is off, those circuits will be turned off and the segment and common output are in high impedance state.

Phase 1 and 2 Period Adjustment (B1h)

This command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 1 to 16 in the unit of DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 1 to 16 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_{PA} , V_{PB} , V_{PC} for color A, B and C respectively.

Set Display Clock Divide Ratio/ Oscillator Frequency (B3h)

This command consists of two functions:

- Display Clock Divide Ratio (A[3:0])
Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with power on reset value = 1. Please refer to section "Oscillator Circuit and Display Time Generator" for the details of DCLK and CLK.
- Oscillator Frequency (A[7:4])
Program the oscillator frequency Fosc which is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency setting available as shown below. The default value is 1101b which represents 0.97MHz Fosc.

Set Gray Scale Table (B8h)

This command is used to set the gray scale table for the display. Except gray scale entry 0, which is zero as it has no pre-charge and current drive, each odd entry gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter is the OLED pixel when it's turned on. Please refer to section "Graphic Display Data RAM (GDDRAM)" for more detailed explanation of relation of display data RAM, gray scale table and the pixel brightness.

Following the command B8h, the user has to set the pulse width from PW1, PW3, PW5, ..., PW59, PW61, PW63 one by one in sequence and complies the following conditions.

$$PW1 > 0; PW3 > PW1 + 1; PW5 > PW3 + 1; \dots$$

Afterwards, the driver automatically derives the pulse width of even entry of gray scale table PW2, PW4, ..., PW62 with the formula like below.

$$PWn = (PW_{n-1} + PW_{n+1}) / 2$$

For example, if PW1 = 3 DCLKs and PW3 = 7 DCLKs, PW2 = (3+7)/2 = 5 DCLKs

The setting of gray scale table entry can perform gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate gray scale table setting like example below can compensate this effect.

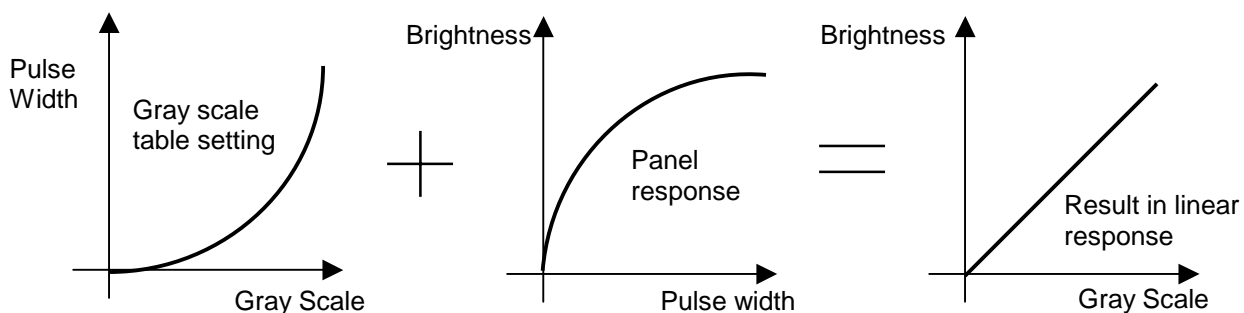


Figure 22 – Example of gamma correction by gray scale table setting

Enable Linear Gray Scale Table (B9h)

This command reloads the preset linear gray scale table as PW1 = 1, PW2 = 3, PW3 = 5, ..., PW62 = 123, PW63 = 125 DCLKs.

Set V_{PA} , V_{PB} and V_{PC} Voltage for Color A, B and C (BBh, BCh and BDh)

These three commands are used to set V_{PA} , V_{PB} and V_{PC} phase 2 voltage level for color A, B and C respectively. The commands are valid in condition that these voltages are selected to generate internally by command ADh. It can be programmed to set the pre-charge voltage reference to V_{REF} or V_{COMH} .

Set V_{COMH} Voltage (BEh)

This command sets the high voltage level of common pins, V_{COMH} , when it is selected to generate internally by command ADh. The level of V_{COMH} is programmed with reference to V_{REF} .

10 GRAPHIC ACCELERATION COMMAND SET DESCRIPTION

Draw Line (21h)

This command draws a line by the given start, end column and row coordinates and the color of the line.

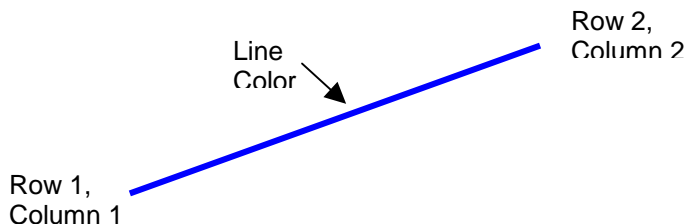


Figure 23 – Example of Draw Line Command

For example, the line above can be drawn by the following command sequence.

1. Enter into draw line mode by command 21h
2. Send column start address of line, column1, for example = 1h
3. Send row start address of line, row 1, for example = 10h
4. Send column end address of line, column 2, for example = 28h
5. Send row end address of line, row 2, for example = 4h
6. Send color C, B and A of line, for example = 35d, 0d, 0d for blue color

Draw Rectangle (22h)

Given the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2), specify the outline and fill area colors, a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.

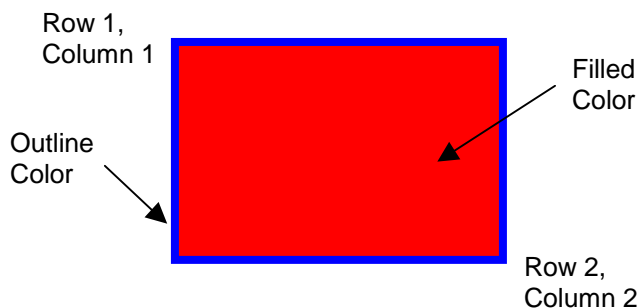


Figure 24 – Example of Draw Rectangle Command

The following example illustrates the rectangle drawing command sequence.

1. Enter the "draw rectangle mode" by execute the command 22h
2. Set the starting column coordinates, Column 1. e.g., 03h.
3. Set the starting row coordinates, Row 1. e.g., 02h.
4. Set the finishing column coordinates, Column 2. e.g., 12h
5. Set the finishing row coordinates, Row 2. e.g., 15h
6. Set the outline color C, B and A. e.g., (28d, 0d, 0d) for blue color
7. Set the filled color C, B and A. e.g., (0d, 0d, 40d) for red color

Copy (23h)

Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

1. Enter the "copy mode" by execute the command 23h
2. Set the starting column coordinates, Column 1. E.g., 00h.
3. Set the starting row coordinates, Row 1. E.g., 00h.
4. Set the finishing column coordinates, Column 2. E.g., 05h
5. Set the finishing row coordinates, Row 2. E.g., 05h
6. Set the new column coordinates, Column 3. E.g., 03h
7. Set the new row coordinates, Row 3. E.g., 03h

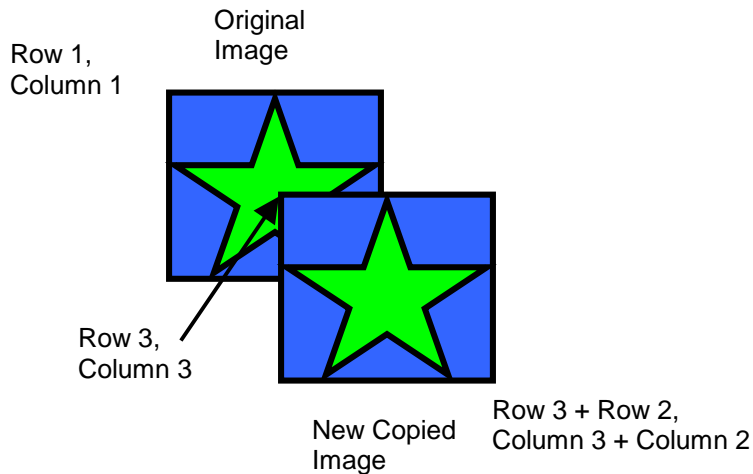


Figure 25 – Example of Copy Command

Dim Window (24h)

This command will dim the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2). After the execution of this command, the selected window area will become darker as follow.

Table 9 – Result of Change of Brightness by Dim Window Command

| Original gray scale | New gray scale after dim window command |
|---------------------|---|
| GS0 ~ GS15 | No change |
| GS16 ~ GS19 | GS4 |
| GS20 ~ GS23 | GS5 |
| : | : |
| GS60 ~ GS63 | GS15 |

Additional execution of this command over the same window area will not change the data content.

Clear Window (25h)

This command sets the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to clear the window display. The graphic display data RAM content of the specified window area will be set to zero.

This command can be combined with Copy command to make as a “move” result. The following example illustrates the copy plus clear procedure and results in moving the window object.

1. Enter the “copy mode” by execute the command 23h
2. Set the starting column coordinates, Column 1. E.g., 00h.
3. Set the starting row coordinates, Row 1. E.g., 00h.
4. Set the finishing column coordinates, Column 2. E.g., 05h
5. Set the finishing row coordinates, Row 2. E.g., 05h
6. Set the new column coordinates, Column 3. E.g., 06h
7. Set the new row coordinates, Row 3. E.g., 06h
8. Enter the “clear mode” by execute the command 24h
9. Set the starting column coordinates, Column 1. E.g., 00h.
10. Set the starting row coordinates, Row 1. E.g., 00h.
11. Set the finishing column coordinates, Column 2. E.g., 05h
12. Set the finishing row coordinates, Row 2. E.g., 05h

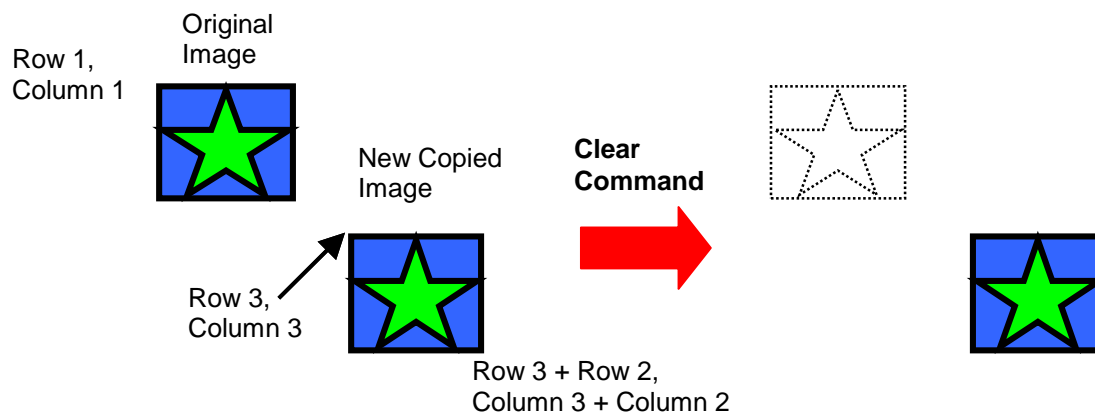


Figure 26 – Example of Copy + Clear = Move Command

Fill Enable/Disable (26h)

This command has two functions.

- Enable/Disable fill (A[0])
 - 0 = Disable filling of color into rectangle in draw rectangle command. (POR)
 - 1 = Enable filling of color into rectangle in draw rectangle command.
- Enable/Disable reverse copy (A[4])
 - 0 = Disable reverse copy (POR)
 - 1 = During copy command, the new image colors are swapped such that “GS0” <-> “GS63”, “GS1” <-> “GS62”,

11 MAXIMUM RATINGS

Table 10 - Maximum Ratings

(Voltage Reference to V_{SS})

| Symbol | Parameter | Value | Unit |
|------------|-------------------------------|------------------------------|------|
| V_{DD} | Supply Voltage | -0.3 to +4 | V |
| V_{CC} | | 0 to 18 | V |
| V_{REF} | | 0 to 18 | V |
| V_{COMH} | Supply Voltage/Output voltage | 0 to 16 | V |
| - | SEG/COM output voltage | 0 to 16 | V |
| V_{in} | Input voltage | $V_{SS}-0.3$ to $V_{DD}+0.3$ | V |
| T_A | Operating Temperature | -40 to +85 | °C |
| T_{stg} | Storage Temperature Range | -65 to +150 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

12 DC CHARACTERISTICS

Table 11 - DC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS} , $V_{DD} = 2.4$ to $3.5V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|-------------|---|---|--------------------|-----------|--------------------|---------|
| V_{CC} | Operating Voltage | | 7 | 11 | 18 | V |
| V_{DD} | Logic Supply Voltage | | 2.4 | 2.7 | 3.5 | V |
| V_{OH} | High Logic Output Level | $I_{out} = 100\mu A$, 3.3MHz | $0.9 \cdot V_{DD}$ | - | V_{DD} | V |
| V_{OL} | Low Logic Output Level | $I_{out} = 100\mu A$, 3.3MHz | 0 | - | $0.1 \cdot V_{DD}$ | V |
| V_{IH} | High Logic Input Level | $I_{out} = 100\mu A$, 3.3MHz | $0.8 \cdot V_{DD}$ | - | V_{DD} | V |
| V_{IL} | Low Logic Input Level | $I_{out} = 100\mu A$, 3.3MHz | 0 | - | $0.2 \cdot V_{DD}$ | V |
| I_{SLEEP} | Sleep mode Current | $V_{DD}=2.7V$, Display OFF, No panel attached | - | - | 5 | μA |
| I_{CC} | V_{CC} Supply Current | $V_{DD}=2.7V$, $V_{CC}=11V$, Display ON Contrast =FF, No panel attached | - | 770 | - | μA |
| I_{DD} | V_{DD} Supply Current | $V_{DD}=2.7V$, $V_{CC}=11V$, Display ON Contrast =FF, No panel attached | - | 170 | - | μA |
| I_{SEG} | Segment Output Current Setting $V_{DD}=2.7V$, $V_{CC}=11V$, $I_{REF}=10\mu A$, All one pattern, Display on, Segment pin under test is connected with a $33K\Omega$ resistive load to V_{CC} . | Contrast = FF | - | 160 | - | μA |
| | | Contrast = AF | - | 110 | - | μA |
| | | Contrast = 5F | - | 60 | - | μA |
| | | Contrast = 00 | - | 0 | - | μA |
| Dev | Segment output current uniformity | $Dev = (I_{SEG} - I_{MID})/I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN})/2$ $I_{SEG}[0:287] =$ Segment current at contrast = FF | - | - | 3 | % |
| Adj. Dev | Adjacent pin output current uniformity (contrast = FF) | $Adj\ Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])$ | - | ± 2.0 | -- | % |
| V_{CC} | Booster output voltage (V_{CC}) | $V_{in}=3V$, $L=22\mu H$; $R1=450K\Omega$; $R2=50K\Omega$; $I_{CC} = 30mA$ (soaking) | 11 | - | 13 | V |
| Pwr | Booster output power | $V_{in}=3V$, $L=22\mu H$; $V_{CC} = 10V \sim 16V$ | - | - | 400 | mW |

13 AC CHARACTERISTICS

Table 12 - AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS} , $V_{DD} = 2.4$ to $3.5V$, $T_A = 25^\circ C$.)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|-----------|---|--|-----|---|-----|------|
| F_{OSC} | Oscillation Frequency of Display Timing Generator | $V_{DD} = 2.7V$ | - | 0.97 | - | MHz |
| F_{FRM} | Frame Frequency for 64 MUX Mode | 96RGB x 64 Graphic Display Mode, Display ON, Internal Oscillator Enabled | - | $F_{OSC} \times \frac{1}{(D \times K \times 64)}$ | - | Hz |

D: divide ratio (POR=1)

K: number of display clocks (POR=136, i.e. phase1 dclk+phase2 dclk+ phase3 dclk=4+7+125)

Table 13 - 6800-Series MPU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = -40$ to $85^{\circ}C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 0 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| PW_{CSL} | Chip Select Low Pulse Width (read) | 120 | - | - | ns |
| | Chip Select Low Pulse Width (write) | 60 | - | - | ns |
| PW_{CSH} | Chip Select High Pulse Width (read) | 60 | - | - | ns |
| | Chip Select High Pulse Width (write) | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

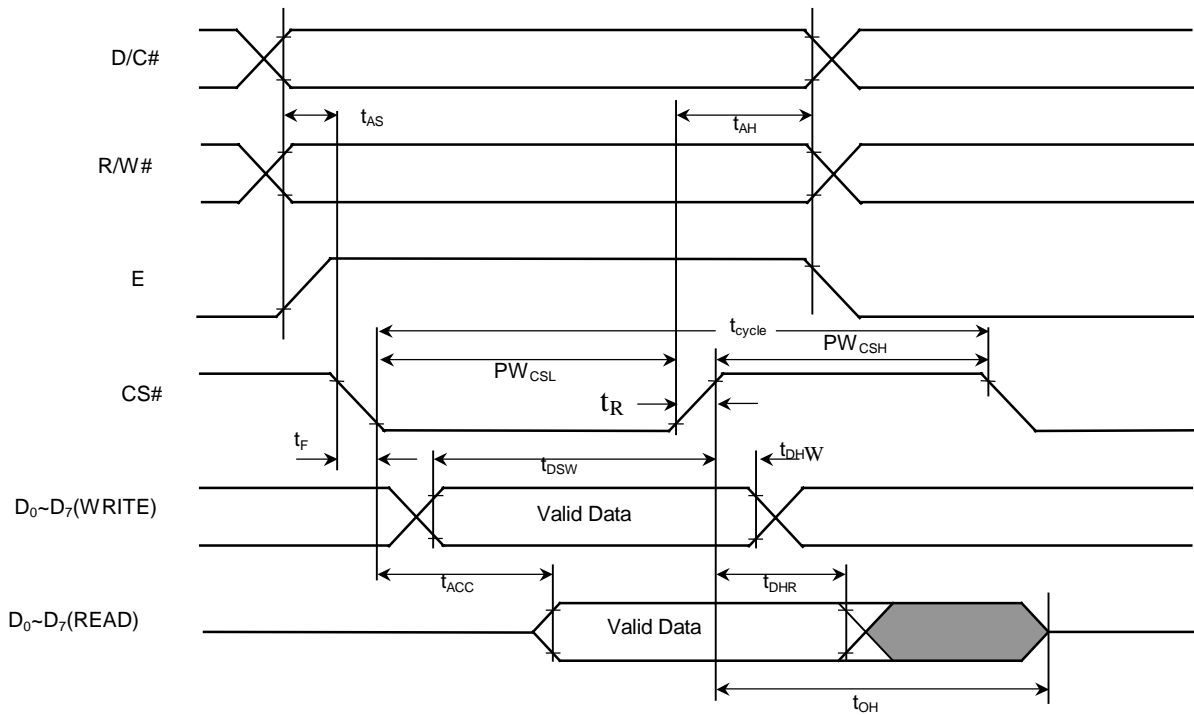


Figure 27 - 6800-series MPU parallel interface characteristics

Table 14 - 8080-Series MPU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = -40$ to $85^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|---|-----------|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 0 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| PW_{CSL} | Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write) | 120 60 | - | - | ns |
| PW_{CSH} | Chip Select High Pulse Width (read) Chip Select High Pulse Width (write) | 60 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

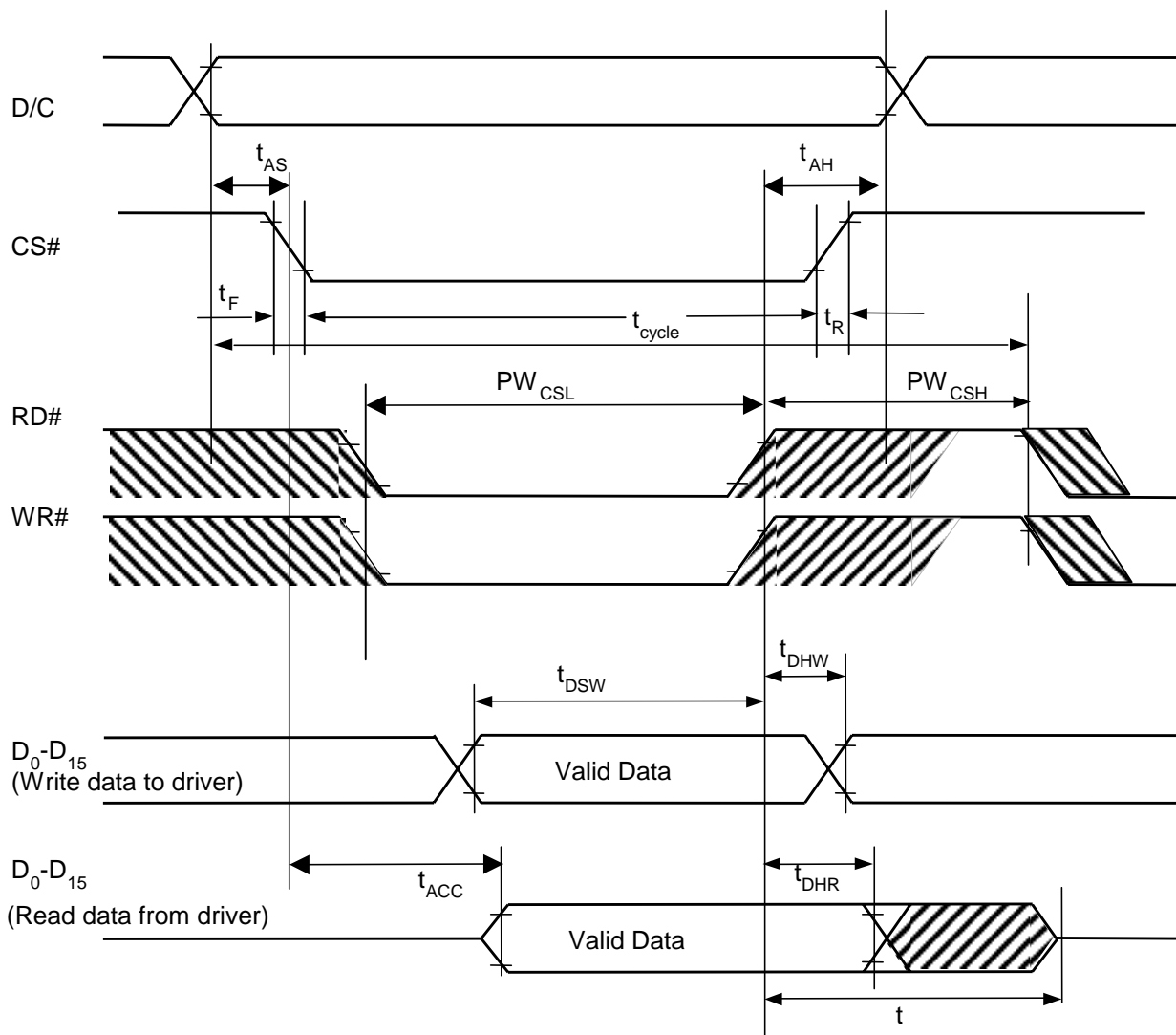


Figure 28 - 8080-series MPU parallel interface characteristics

Table 15 - Serial Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = -40$ to $85^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 250 | - | - | ns |
| t_{AS} | Address Setup Time | 150 | - | - | ns |
| t_{AH} | Address Hold Time | 150 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 120 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 60 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 100 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 100 | - | - | ns |
| t_{CLKL} | Clock Low Time | 100 | - | - | ns |
| t_{CLKH} | Clock High Time | 100 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

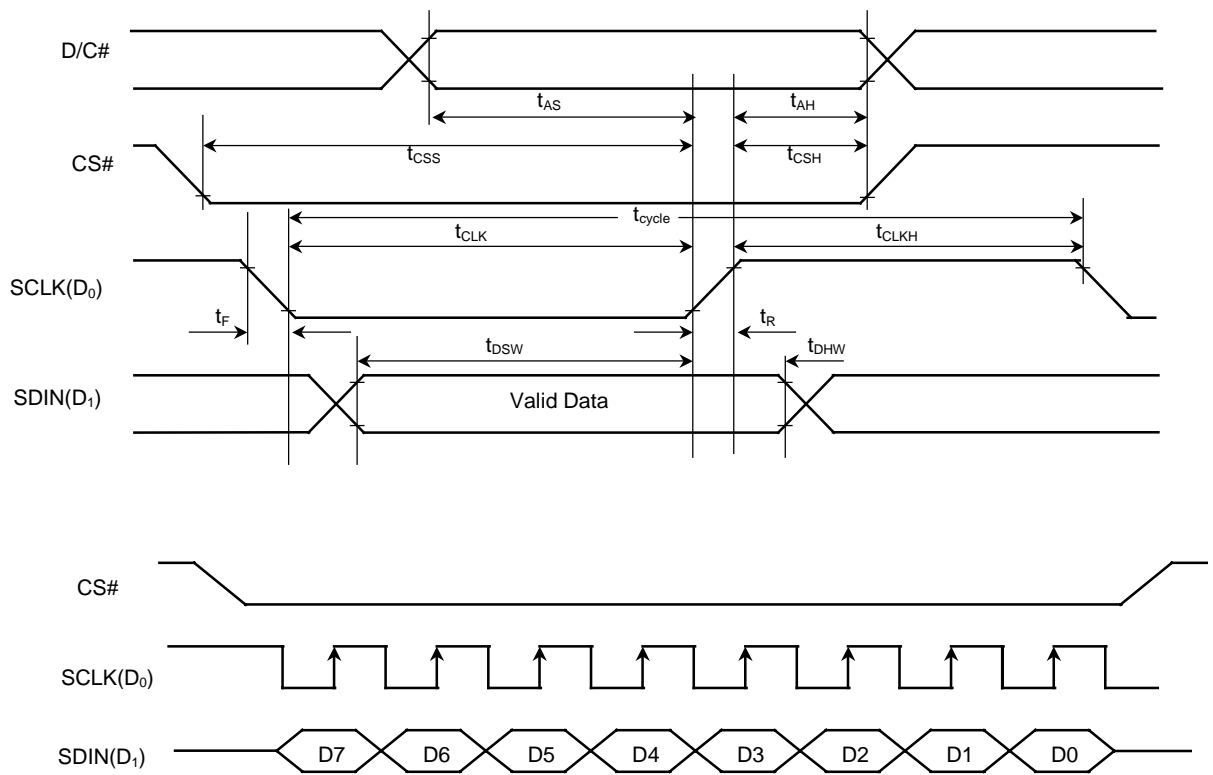
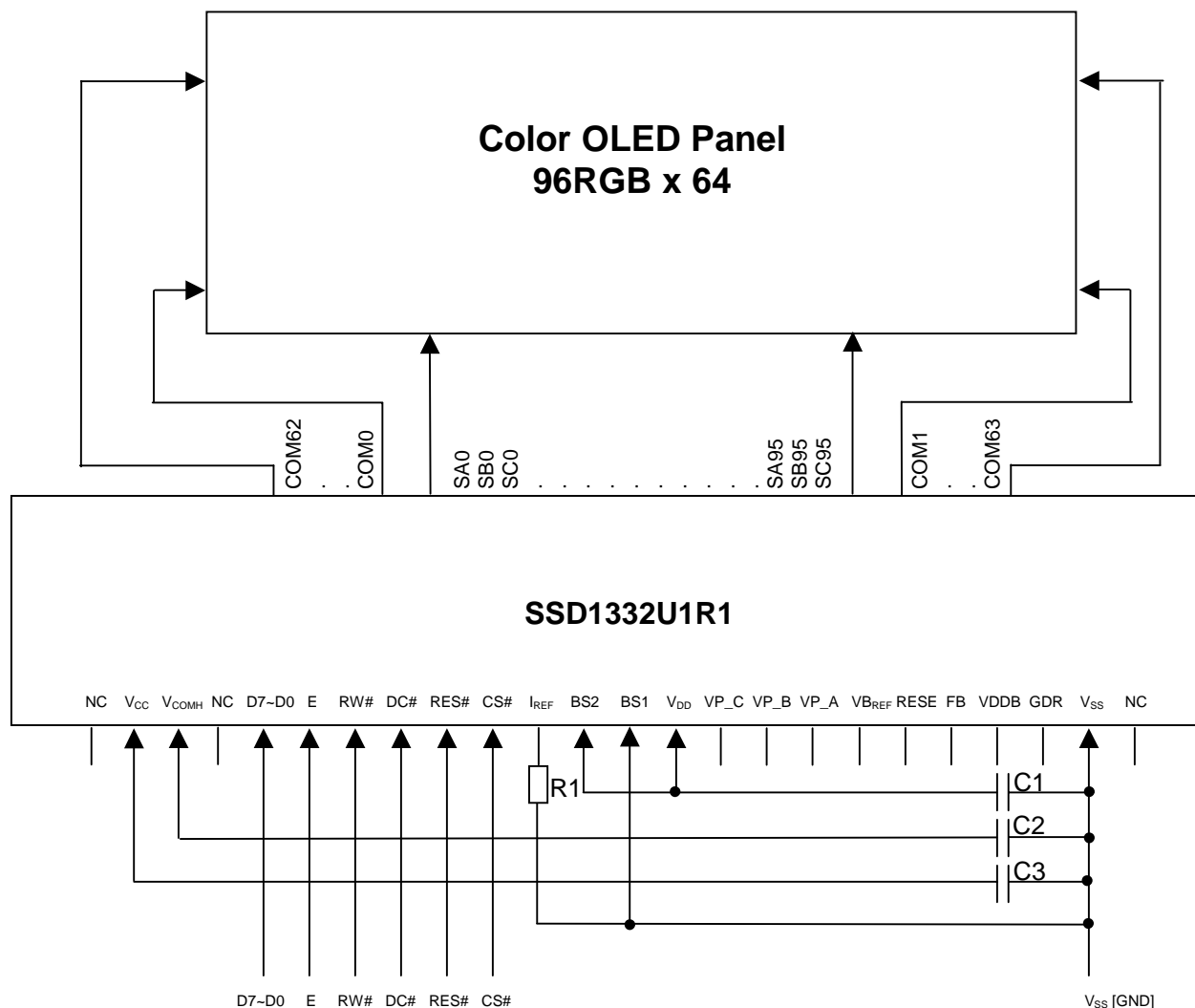


Figure 29 - Serial interface characteristics

14 APPLICATION EXAMPLE

The configuration for 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
 ($V_{DD} = 3.0V$, external $V_{CC} = 12V$, $I_{REF} = 10\mu A$)



Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, RES#, CS#
 Pin internally connected to V_{DD} : M/S#, CLS
 Pin internally connected to V_{SS} : VSSB
 Pin internally connected to V_{CC} : VREF
 Pin externally connected to V_{DD} : BS2
 Pin externally connected to V_{SS} : BS1
 Pin floated: VP_C, VP_B, VP_A, VBREF, RESE, FB, VDDB, GDR

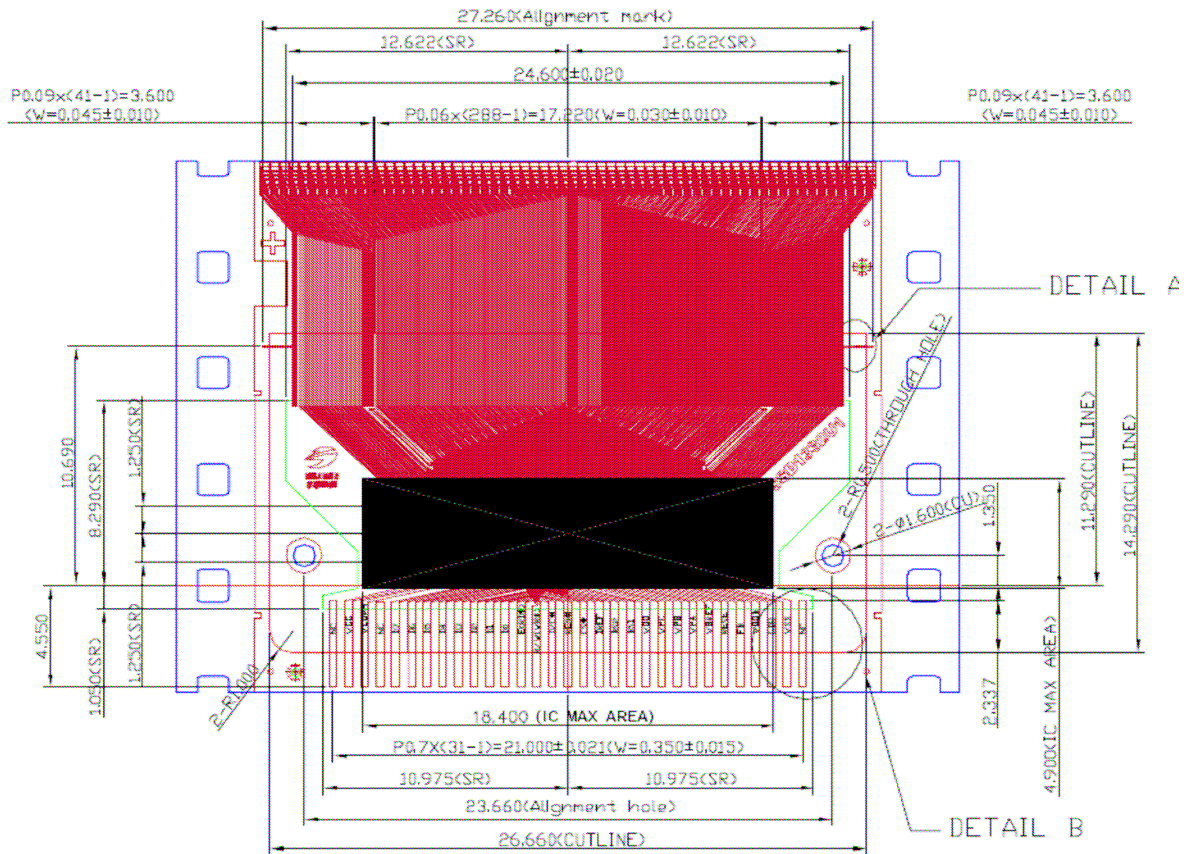
C1~C3: 4.7uF
 Voltage at $I_{REF} = V_{CC} - 3V$
 $R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} = 910K\Omega$

Figure 30 - Application Example for SSD1332U1R1

15 SSD1332U1R1 COF PACKAGE DIMENSIONS

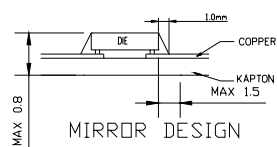
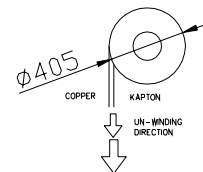


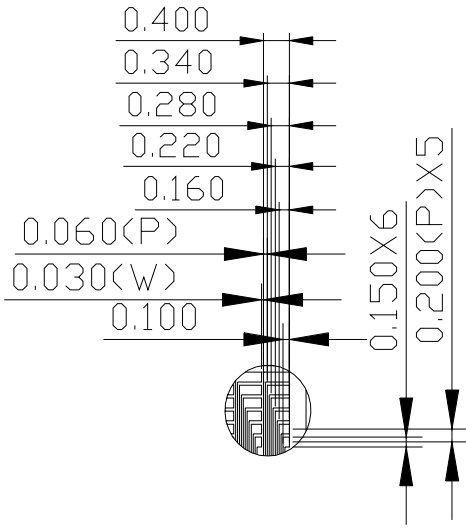
TAPE
UN-WINDING
DIRECTION



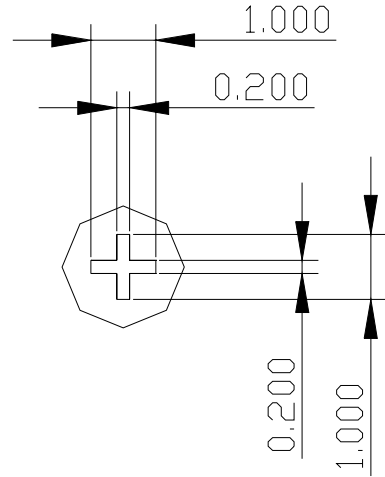
NOTE:

1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
 - PI: KAPTON (150EN) 38±4um
 - CU: 8±2um
 - SR: SN9000 15±10um
 - (OTHER TOLERANCE: ±0.200)
3. SN PLATING: 0.15±0.05um
4. TAP SITE: 5 SPH, 23.75mm

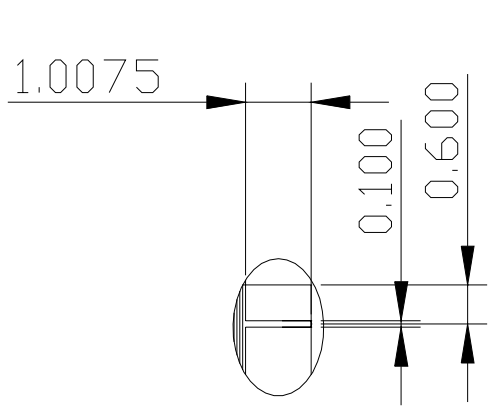




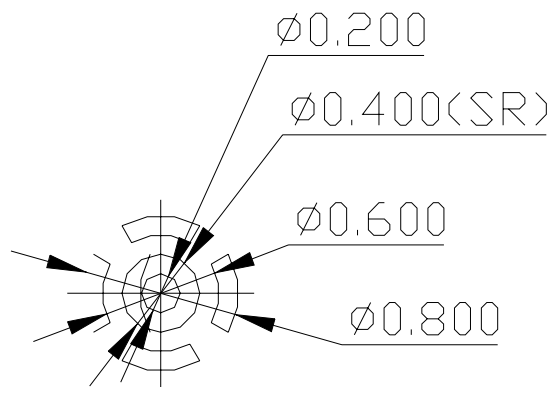
DETAIL A:
TEST PAD



DETAIL B



DETAIL C



SR ALIGNMENT MARK
SCALE 3:1

16 SSD1332U1R1 COF PIN ASSIGNMENT

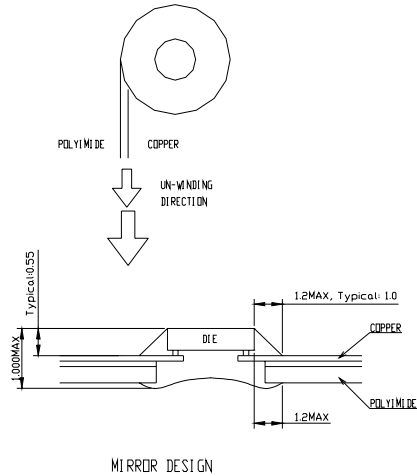
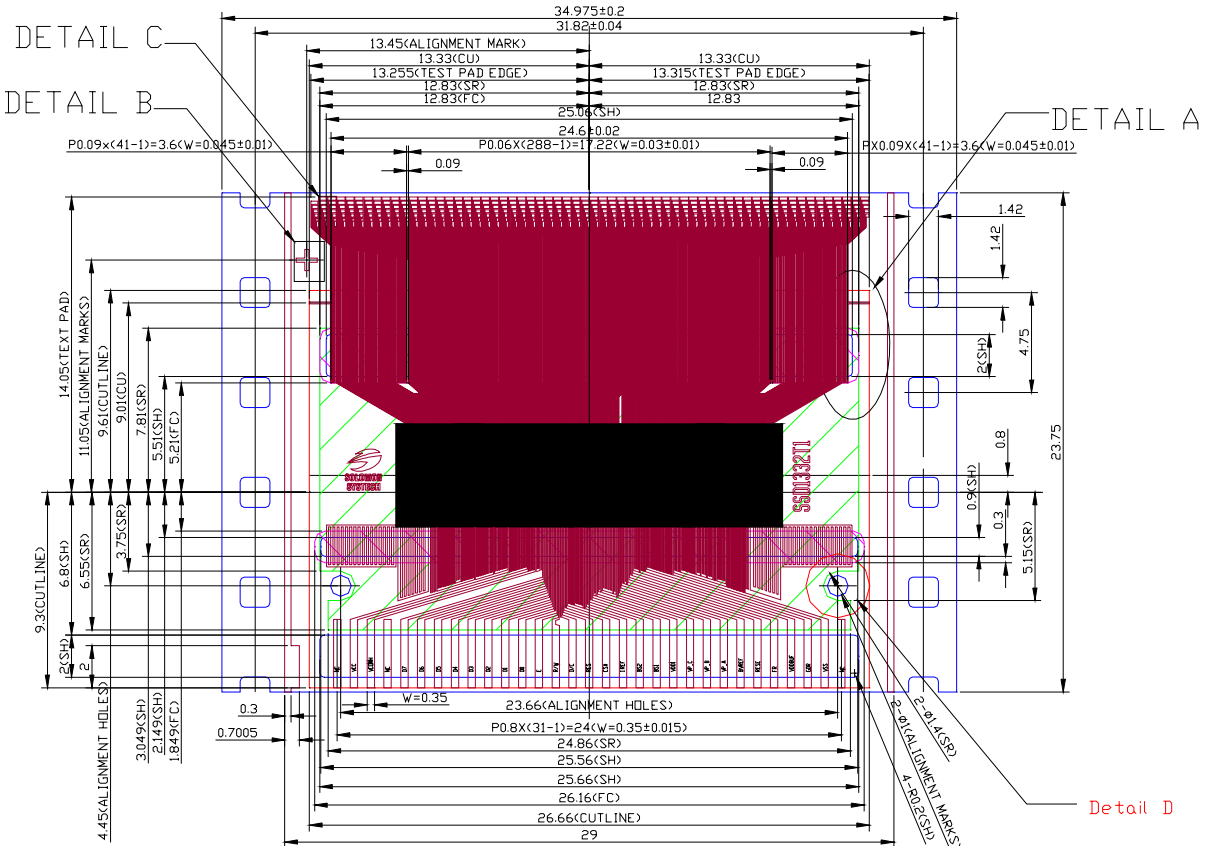
| | | | |
|----|--------|-----|-------|
| 1 | NC | 401 | NC |
| 2 | VCC | 400 | NC |
| 3 | VCOMH | 399 | NC |
| 4 | NC | 398 | COM62 |
| 5 | D7 | 397 | COM60 |
| 6 | D6 | 396 | COM58 |
| 7 | D5 | | |
| 8 | D4 | | |
| 9 | D3 | 369 | COM4 |
| 10 | D2 | 368 | COM2 |
| 11 | D1 | 367 | COM0 |
| 12 | D0 | 366 | NC |
| 13 | E<RD> | 365 | NC |
| 14 | RW#<WR | 364 | NC |
| 15 | DC# | 363 | NC |
| 16 | RES# | 362 | NC |
| 17 | CS# | 361 | NC |
| 18 | IREF | 360 | SA0 |
| 19 | BS2 | 359 | SB0 |
| 20 | BS1 | 358 | SC0 |
| 21 | VDD | | |
| 22 | VP_C | 75 | SA95 |
| 23 | VP_B | 74 | SB95 |
| 24 | VP_A | 73 | SC95 |
| 25 | VBREF | 72 | NC |
| 26 | RESE | 71 | NC |
| 27 | FB | 70 | NC |
| 28 | VDDDB | 69 | NC |
| 29 | GDR | 68 | NC |
| 30 | VSS | 67 | NC |
| 31 | NC | 66 | COM1 |
| | | 65 | COM3 |
| | | 64 | COM5 |
| | | | |
| | | 37 | ROW59 |
| | | 36 | ROW61 |
| | | 35 | COM63 |
| | | 34 | NC |
| | | 33 | NC |
| | | 32 | NC |

Figure 31 - SSD1332U1R1 COF pin assignment

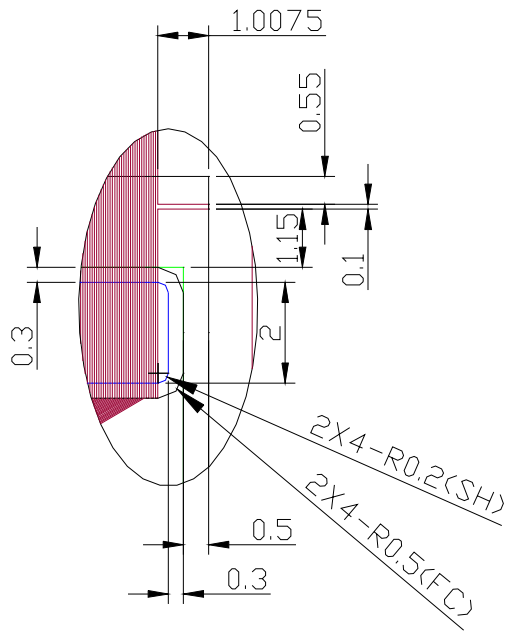
| Pin # | Pin name | Pin # | Pin name | Pin # | Pin name | Pin # | Pin name | Pin # | Pin name |
|-------|-----------|-------|----------|-------|----------|-------|----------|-------|----------|
| 1 | NC | 81 | SA93 | 161 | SB66 | 241 | SC39 | 321 | SA13 |
| 2 | VCC | 82 | SC92 | 162 | SA66 | 242 | SB39 | 322 | SC12 |
| 3 | VCOMH | 83 | SB92 | 163 | SC65 | 243 | SA39 | 323 | SB12 |
| 4 | NC | 84 | SA92 | 164 | SB65 | 244 | SC38 | 324 | SA12 |
| 5 | D7 | 85 | SC91 | 165 | SA65 | 245 | SB38 | 325 | SC11 |
| 6 | D6 | 86 | SB91 | 166 | SC64 | 246 | SA38 | 326 | SB11 |
| 7 | D5 | 87 | SA91 | 167 | SB64 | 247 | SC37 | 327 | SA11 |
| 8 | D4 | 88 | SC90 | 168 | SA64 | 248 | SB37 | 328 | SC10 |
| 9 | D3 | 89 | SB90 | 169 | SC63 | 249 | SA37 | 329 | SB10 |
| 10 | D2 | 90 | SA90 | 170 | SB63 | 250 | SC36 | 330 | SA10 |
| 11 | D1 | 91 | SC89 | 171 | SA63 | 251 | SB36 | 331 | SC9 |
| 12 | D0 | 92 | SB89 | 172 | SC62 | 252 | SA36 | 332 | SB9 |
| 13 | E(RD#) | 93 | SA89 | 173 | SB62 | 253 | SC35 | 333 | SA9 |
| 14 | R/W#(WR#) | 94 | SC88 | 174 | SA62 | 254 | SB35 | 334 | SC8 |
| 15 | D/C# | 95 | SB88 | 175 | SC61 | 255 | SA35 | 335 | SB8 |
| 16 | RES | 96 | SA88 | 176 | SB61 | 256 | SC34 | 336 | SA8 |
| 17 | CS# | 97 | SC87 | 177 | SA61 | 257 | SB34 | 337 | SC7 |
| 18 | IREF | 98 | SB87 | 178 | SC60 | 258 | SA34 | 338 | SB7 |
| 19 | BS2 | 99 | SA87 | 179 | SB60 | 259 | SC33 | 339 | SA7 |
| 20 | BS1 | 100 | SC86 | 180 | SA60 | 260 | SB33 | 340 | SC6 |
| 21 | VDD | 101 | SB86 | 181 | SC59 | 261 | SA33 | 341 | SB6 |
| 22 | VP_C | 102 | SA86 | 182 | SB59 | 262 | SC32 | 342 | SA6 |
| 23 | VP_B | 103 | SC85 | 183 | SA59 | 263 | SB32 | 343 | SC5 |
| 24 | VP_A | 104 | SB85 | 184 | SC58 | 264 | SA32 | 344 | SB5 |
| 25 | VBREF | 105 | SA85 | 185 | SB58 | 265 | SC31 | 345 | SA5 |
| 26 | RESE | 106 | SC84 | 186 | SA58 | 266 | SB31 | 346 | SC4 |
| 27 | FB | 107 | SB84 | 187 | SC57 | 267 | SA31 | 347 | SB4 |
| 28 | VDDB | 108 | SA84 | 188 | SB57 | 268 | SC30 | 348 | SA4 |
| 29 | GDR | 109 | SC83 | 189 | SA57 | 269 | SB30 | 349 | SC3 |
| 30 | VSS | 110 | SB83 | 190 | SC56 | 270 | SA30 | 350 | SB3 |
| 31 | NC | 111 | SA83 | 191 | SB56 | 271 | SC29 | 351 | SA3 |
| 32 | NC | 112 | SC82 | 192 | SA56 | 272 | SB29 | 352 | SC2 |
| 33 | NC | 113 | SB82 | 193 | SC55 | 273 | SA29 | 353 | SB2 |
| 34 | NC | 114 | SA82 | 194 | SB55 | 274 | SC28 | 354 | SA2 |
| 35 | COM63 | 115 | SC81 | 195 | SA55 | 275 | SB28 | 355 | SC1 |
| 36 | COM61 | 116 | SB81 | 196 | SC54 | 276 | SA28 | 356 | SB1 |
| 37 | COM59 | 117 | SA81 | 197 | SB54 | 277 | SC27 | 357 | SA1 |
| 38 | COM57 | 118 | SC80 | 198 | SA54 | 278 | SB27 | 358 | SC0 |
| 39 | COM55 | 119 | SB80 | 199 | SC53 | 279 | SA27 | 359 | SB0 |
| 40 | COM53 | 120 | SA80 | 200 | SB53 | 280 | SC26 | 360 | SA0 |
| 41 | COM51 | 121 | SC79 | 201 | SA53 | 281 | SB26 | 361 | NC |
| 42 | COM49 | 122 | SB79 | 202 | SC52 | 282 | SA26 | 362 | NC |
| 43 | COM47 | 123 | SA79 | 203 | SB52 | 283 | SC25 | 363 | NC |
| 44 | COM45 | 124 | SC78 | 204 | SA52 | 284 | SB25 | 364 | NC |
| 45 | COM43 | 125 | SB78 | 205 | SC51 | 285 | SA25 | 365 | NC |
| 46 | COM41 | 126 | SA78 | 206 | SB51 | 286 | SC24 | 366 | NC |
| 47 | COM39 | 127 | SC77 | 207 | SA51 | 287 | SB24 | 367 | COM0 |
| 48 | COM37 | 128 | SB77 | 208 | SC50 | 288 | SA24 | 368 | COM2 |
| 49 | COM35 | 129 | SA77 | 209 | SB50 | 289 | SC23 | 369 | COM4 |
| 50 | COM33 | 130 | SC76 | 210 | SA50 | 290 | SB23 | 370 | COM6 |
| 51 | COM31 | 131 | SB76 | 211 | SC49 | 291 | SA23 | 371 | COM8 |
| 52 | COM29 | 132 | SA76 | 212 | SB49 | 292 | SC22 | 372 | COM10 |
| 53 | COM27 | 133 | SC75 | 213 | SA49 | 293 | SB22 | 373 | COM12 |
| 54 | COM25 | 134 | SB75 | 214 | SC48 | 294 | SA22 | 374 | COM14 |
| 55 | COM23 | 135 | SA75 | 215 | SB48 | 295 | SC21 | 375 | COM16 |
| 56 | COM21 | 136 | SC74 | 216 | SA48 | 296 | SB21 | 376 | COM18 |
| 57 | COM19 | 137 | SB74 | 217 | SC47 | 297 | SA21 | 377 | COM20 |
| 58 | COM17 | 138 | SA74 | 218 | SB47 | 298 | SC20 | 378 | COM22 |
| 59 | COM15 | 139 | SC73 | 219 | SA47 | 299 | SB20 | 379 | COM24 |
| 60 | COM13 | 140 | SB73 | 220 | SC46 | 300 | SA20 | 380 | COM26 |
| 61 | COM11 | 141 | SA73 | 221 | SB46 | 301 | SC19 | 381 | COM28 |
| 62 | COM9 | 142 | SC72 | 222 | SA46 | 302 | SB19 | 382 | COM30 |
| 63 | COM7 | 143 | SB72 | 223 | SC45 | 303 | SA19 | 383 | COM32 |
| 64 | COM5 | 144 | SA72 | 224 | SB45 | 304 | SC18 | 384 | COM34 |
| 65 | COM3 | 145 | SC71 | 225 | SA45 | 305 | SB18 | 385 | COM36 |
| 66 | COM1 | 146 | SB71 | 226 | SC44 | 306 | SA18 | 386 | COM38 |
| 67 | NC | 147 | SA71 | 227 | SB44 | 307 | SC17 | 387 | COM40 |
| 68 | NC | 148 | SC70 | 228 | SA44 | 308 | SB17 | 388 | COM42 |
| 69 | NC | 149 | SB70 | 229 | SC43 | 309 | SA17 | 389 | COM44 |
| 70 | NC | 150 | SA70 | 230 | SB43 | 310 | SC16 | 390 | COM46 |
| 71 | NC | 151 | SC69 | 231 | SA43 | 311 | SB16 | 391 | COM48 |
| 72 | NC | 152 | SB69 | 232 | SC42 | 312 | SA16 | 392 | COM50 |
| 73 | SC95 | 153 | SA69 | 233 | SB42 | 313 | SC15 | 393 | COM52 |
| 74 | SB95 | 154 | SC68 | 234 | SA42 | 314 | SB15 | 394 | COM54 |
| 75 | SA95 | 155 | SB68 | 235 | SC41 | 315 | SA15 | 395 | COM56 |
| 76 | SC94 | 156 | SA68 | 236 | SB41 | 316 | SC14 | 396 | COM58 |
| 77 | SB94 | 157 | SC67 | 237 | SA41 | 317 | SB14 | 397 | COM60 |
| 78 | SA94 | 158 | SB67 | 238 | SC40 | 318 | SA14 | 398 | COM62 |
| 79 | SC93 | 159 | SA67 | 239 | SB40 | 319 | SC13 | 399 | NC |
| 80 | SB93 | 160 | SC66 | 240 | SA40 | 320 | SB13 | 400 | NC |
| | | | | | | | | 401 | NC |

Table 16 - SSD1332U1R1 COF pin assignment

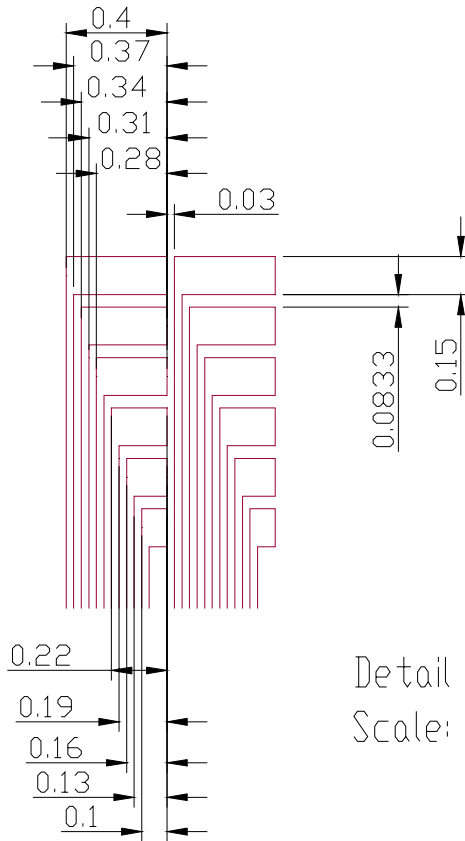
17 SSD1332T1R1 TAB PACKAGE DIMENSIONS



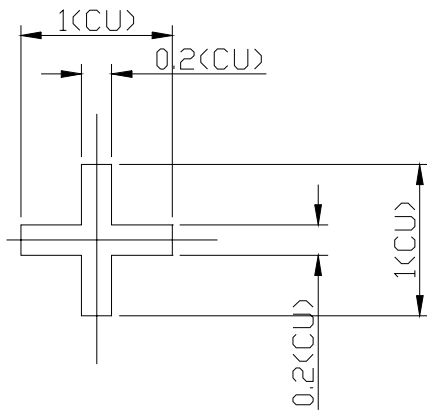
- NOTE:
- GENERAL TOLERANCE: ±0.05mm
 - CUTLINE TOLERANCE: ±0.15mm
 - MATERIAL
 - PI: 75±6UM
 - CU: 15um
 - SR: 15±10um
 - (OTHER TOLERANCE: ±0.200)
 - SN PLATING: 0.20±0.05um
 - TAP SITE: 5 SPH, 23.75mm



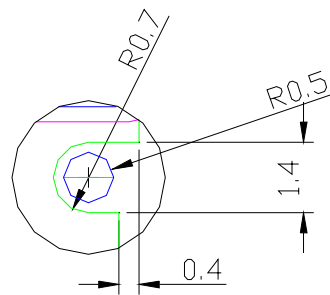
Detail A



Detail C
Scale: 5:1



Detail B
Scale: 3:1



Detail D

18 SSD1332T1R1 TAB PIN ASSIGNMENT

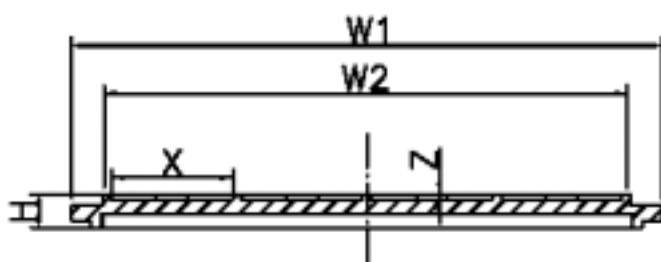
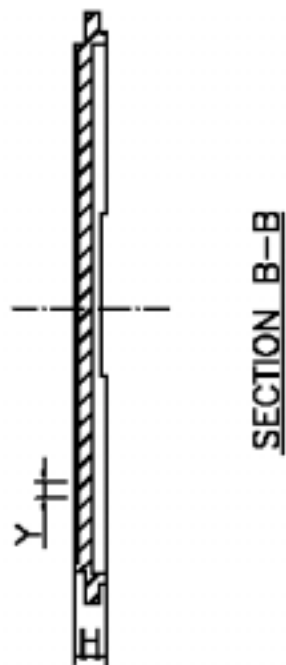
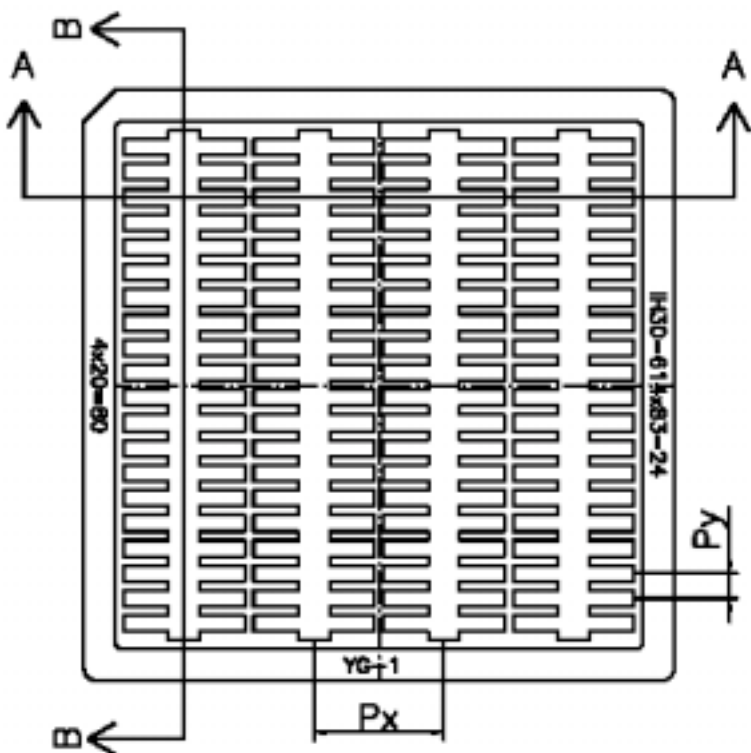
Figure 32 - SSD1332T1R1 TAB pin assignment

| | | | |
|----|-------|-----|-------|
| 1 | NC | 401 | NC |
| 2 | VCC | 400 | NC |
| 3 | VCOMH | 399 | NC |
| 4 | NC | 398 | COM62 |
| 5 | D7 | 397 | COM60 |
| 6 | D6 | 396 | COM58 |
| 7 | D5 | | |
| 8 | D4 | 369 | COM4 |
| 9 | D3 | 368 | COM2 |
| 10 | D2 | 367 | COM0 |
| 11 | D1 | 366 | NC |
| 12 | D0 | 365 | NC |
| 13 | E | 364 | NC |
| 14 | R/W | 363 | NC |
| 15 | D/C | 362 | NC |
| 16 | RES# | 361 | NC |
| 17 | CS# | 360 | SA0 |
| 18 | IREF | 359 | SB0 |
| 19 | BS2 | 358 | SC0 |
| 20 | BS1 | | |
| 21 | VDD | 75 | SA95 |
| 22 | VP_C | 74 | SB95 |
| 23 | VP_B | 73 | SC95 |
| 24 | VP_A | 72 | NC |
| 25 | BVREF | 71 | NC |
| 26 | RESE | 70 | NC |
| 27 | FR | 69 | NC |
| 28 | VDDB | 68 | NC |
| 29 | GDR | 67 | NC |
| 30 | VSS | 66 | COM1 |
| 31 | NC | 65 | COM3 |
| | | 64 | COM5 |
| | | 37 | COM61 |
| | | 36 | COM63 |
| | | 35 | NC |
| | | 34 | NC |
| | | 33 | NC |
| | | 32 | NC |

| Pad.no | Pad.name | Pad.no | Pad.name | Pad.no | Pad.name | Pad.no | Pad.name | Pad.no | Pad.name | Pad.no | Pad.name | Pad.no | Pad.name |
|--------|----------|--------|----------|--------|----------|--------|----------|--------|----------|--------|----------|--------|----------|
| 1 | NC | 61 | COM11 | 121 | SC79 | 181 | SC59 | 241 | SC39 | 301 | SC19 | 361 | NC |
| 2 | VCC | 62 | COM9 | 122 | SB79 | 182 | SB59 | 242 | SB39 | 302 | SB19 | 362 | NC |
| 3 | VCOMH | 63 | COM7 | 123 | SA79 | 183 | SA59 | 243 | SA39 | 303 | SA19 | 363 | NC |
| 4 | NC | 64 | COM5 | 124 | SC78 | 184 | SC58 | 244 | SC38 | 304 | SC18 | 364 | NC |
| 5 | D7 | 65 | COM3 | 125 | SB78 | 185 | SB58 | 245 | SB38 | 305 | SB18 | 365 | NC |
| 6 | D6 | 66 | COM1 | 126 | SA78 | 186 | SA58 | 246 | SA38 | 306 | SA18 | 366 | NC |
| 7 | D5 | 67 | NC | 127 | SC77 | 187 | SC57 | 247 | SC37 | 307 | SC17 | 367 | COM0 |
| 8 | D4 | 68 | NC | 128 | SB77 | 188 | SB57 | 248 | SB37 | 308 | SB17 | 368 | COM2 |
| 9 | D3 | 69 | NC | 129 | SA77 | 189 | SA57 | 249 | SA37 | 309 | SA17 | 369 | COM4 |
| 10 | D2 | 70 | NC | 130 | SC76 | 190 | SC56 | 250 | SC36 | 310 | SC16 | 370 | COM6 |
| 11 | D1 | 71 | NC | 131 | SB76 | 191 | SB56 | 251 | SB36 | 311 | SB16 | 371 | COM8 |
| 12 | D0 | 72 | NC | 132 | SA76 | 192 | SA56 | 252 | SA36 | 312 | SA16 | 372 | COM10 |
| 13 | E | 73 | SC95 | 133 | SC75 | 193 | SC55 | 253 | SC35 | 313 | SC15 | 373 | COM12 |
| 14 | R/W | 74 | SB95 | 134 | SB75 | 194 | SB55 | 254 | SB35 | 314 | SB15 | 374 | COM14 |
| 15 | D/C | 75 | SA95 | 135 | SA75 | 195 | SA55 | 255 | SA35 | 315 | SA15 | 375 | COM16 |
| 16 | RES# | 76 | SC94 | 136 | SC74 | 196 | SC54 | 256 | SC34 | 316 | SC14 | 376 | COM18 |
| 17 | CS# | 77 | SB94 | 137 | SB74 | 197 | SB54 | 257 | SB34 | 317 | SB14 | 377 | COM20 |
| 18 | IREF | 78 | SA94 | 138 | SA74 | 198 | SA54 | 258 | SA34 | 318 | SA14 | 378 | COM22 |
| 19 | BS2 | 79 | SC93 | 139 | SC73 | 199 | SC53 | 259 | SC33 | 319 | SC13 | 379 | COM24 |
| 20 | BS1 | 80 | SB93 | 140 | SB73 | 200 | SB53 | 260 | SB33 | 320 | SB13 | 380 | COM26 |
| 21 | VDD | 81 | SA93 | 141 | SA73 | 201 | SA53 | 261 | SA33 | 321 | SA13 | 381 | COM28 |
| 22 | VP_C | 82 | SC92 | 142 | SC72 | 202 | SC52 | 262 | SC32 | 322 | SC12 | 382 | COM30 |
| 23 | VP_B | 83 | SB92 | 143 | SB72 | 203 | SB52 | 263 | SB32 | 323 | SB12 | 383 | COM32 |
| 24 | VP_A | 84 | SA92 | 144 | SA72 | 204 | SA52 | 264 | SA32 | 324 | SA12 | 384 | COM34 |
| 25 | BVREF | 85 | SC91 | 145 | SC71 | 205 | SC51 | 265 | SC31 | 325 | SC11 | 385 | COM36 |
| 26 | RESE | 86 | SB91 | 146 | SB71 | 206 | SB51 | 266 | SB31 | 326 | SB11 | 386 | COM38 |
| 27 | FR | 87 | SA91 | 147 | SA71 | 207 | SA51 | 267 | SA31 | 327 | SA11 | 387 | COM40 |
| 28 | VDDB | 88 | SC90 | 148 | SC70 | 208 | SC50 | 268 | SC30 | 328 | SC10 | 388 | COM42 |
| 29 | GDR | 89 | SB90 | 149 | SB70 | 209 | SB50 | 269 | SB30 | 329 | SB10 | 389 | COM44 |
| 30 | VSS | 90 | SA90 | 150 | SA70 | 210 | SA50 | 270 | SA30 | 330 | SA10 | 390 | COM46 |
| 31 | NC | 91 | SC89 | 151 | SC69 | 211 | SC49 | 271 | SC29 | 331 | SC9 | 391 | COM48 |
| 32 | NC | 92 | SB89 | 152 | SB69 | 212 | SB49 | 272 | SB29 | 332 | SB9 | 392 | COM50 |
| 33 | NC | 93 | SA89 | 153 | SA69 | 213 | SA49 | 273 | SA29 | 333 | SA9 | 393 | COM52 |
| 34 | NC | 94 | SC88 | 154 | SC68 | 214 | SC48 | 274 | SC28 | 334 | SC8 | 394 | COM54 |
| 35 | COM63 | 95 | SB88 | 155 | SB68 | 215 | SB48 | 275 | SB28 | 335 | SB8 | 395 | COM56 |
| 36 | COM61 | 96 | SA88 | 156 | SA68 | 216 | SA48 | 276 | SA28 | 336 | SA8 | 396 | COM58 |
| 37 | COM59 | 97 | SC87 | 157 | SC67 | 217 | SC47 | 277 | SC27 | 337 | SC7 | 397 | COM60 |
| 38 | COM57 | 98 | SB87 | 158 | SB67 | 218 | SB47 | 278 | SB27 | 338 | SB7 | 398 | COM62 |
| 39 | COM55 | 99 | SA87 | 159 | SA67 | 219 | SA47 | 279 | SA27 | 339 | SA7 | 399 | NC |
| 40 | COM53 | 100 | SC86 | 160 | SC66 | 220 | SC46 | 280 | SC26 | 340 | SC6 | 400 | NC |
| 41 | COM51 | 101 | SB86 | 161 | SB66 | 221 | SB46 | 281 | SB26 | 341 | SB6 | 401 | NC |
| 42 | COM49 | 102 | SA86 | 162 | SA66 | 222 | SA46 | 282 | SA26 | 342 | SA6 | | |
| 43 | COM47 | 103 | SC85 | 163 | SC65 | 223 | SC45 | 283 | SC25 | 343 | SC5 | | |
| 44 | COM45 | 104 | SB85 | 164 | SB65 | 224 | SB45 | 284 | SB25 | 344 | SB5 | | |
| 45 | COM43 | 105 | SA85 | 165 | SA65 | 225 | SA45 | 285 | SA25 | 345 | SA5 | | |
| 46 | COM41 | 106 | SC84 | 166 | SC64 | 226 | SC44 | 286 | SC24 | 346 | SC4 | | |
| 47 | COM39 | 107 | SB84 | 167 | SB64 | 227 | SB44 | 287 | SB24 | 347 | SB4 | | |
| 48 | COM37 | 108 | SA84 | 168 | SA64 | 228 | SA44 | 288 | SA24 | 348 | SA4 | | |
| 49 | COM35 | 109 | SC83 | 169 | SC63 | 229 | SC43 | 289 | SC23 | 349 | SC3 | | |
| 50 | COM33 | 110 | SB83 | 170 | SB63 | 230 | SB43 | 290 | SB23 | 350 | SB3 | | |
| 51 | COM31 | 111 | SA83 | 171 | SA63 | 231 | SA43 | 291 | SA23 | 351 | SA3 | | |
| 52 | COM29 | 112 | SC82 | 172 | SC62 | 232 | SC42 | 292 | SC22 | 352 | SC2 | | |
| 53 | COM27 | 113 | SB82 | 173 | SB62 | 233 | SB42 | 293 | SB22 | 353 | SB2 | | |
| 54 | COM25 | 114 | SA82 | 174 | SA62 | 234 | SA42 | 294 | SA22 | 354 | SA2 | | |
| 55 | COM23 | 115 | SC81 | 175 | SC61 | 235 | SC41 | 295 | SC21 | 355 | SC1 | | |
| 56 | COM21 | 116 | SB81 | 176 | SB61 | 236 | SB41 | 296 | SB21 | 356 | SB1 | | |
| 57 | COM19 | 117 | SA81 | 177 | SA61 | 237 | SA41 | 297 | SA21 | 357 | SA1 | | |
| 58 | COM17 | 118 | SC80 | 178 | SC60 | 238 | SC40 | 298 | SC20 | 358 | SC0 | | |
| 59 | COM15 | 119 | SB80 | 179 | SB60 | 239 | SB40 | 299 | SB20 | 359 | SB0 | | |
| 60 | COM13 | 120 | SA80 | 180 | SA60 | 240 | SA40 | 300 | SA20 | 360 | SA0 | | |

Table 17 - SSD1332T1R1 TAB pin assignment

19 SSD1332Z PACKAGE DETAILS



SECTION A-A

| | Spec | |
|-----------|----------------|--------|
| | mm | (mil) |
| W1 | 76.0 +0.2/-0.1 | (2992) |
| W2 | 68.0 +0.2/-0.1 | (2677) |
| H | 4.20 +/-0.1 | (165) |
| Px | 20.36 +/-0.1 | (802) |
| Py | 3.23 +/-0.1 | (127) |
| X | 15.60 +/- | (614) |
| Y | 2.10 +/- | (83) |
| Z | 0.61 +/-0.05 | (24) |
| N | 80 | |

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